AwaXe_v4 TID report

1 Objective

Report of the AwaXe_v4 total ionizing dose (TID) characterization.

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2 List of modifications

3 Applicable and reference documents

Applicable Documents (AD)			
AD	**Title**	**Reference**	**Version**
AD-01	AwaXe_v4 TID testplan	AwaXe-v4-TID-testplan	1.0

Reference Documents (RD)			
RD	**Title**	**Reference**	**Version**
RD-01	AwaXe_v4 datasheet	WFEE-ASIC-AwaXe_v4	1.0
RD-02	AwaXe_v4 developments board	015-AwaXe_v4-3	2022-09-21
RD-03	Fraunhofer TID test report	NEO-23-019_Report_029-2024_v1.0	1.0
RD-04	HDMI board	HDMI board schematic	1.0

4 Introduction

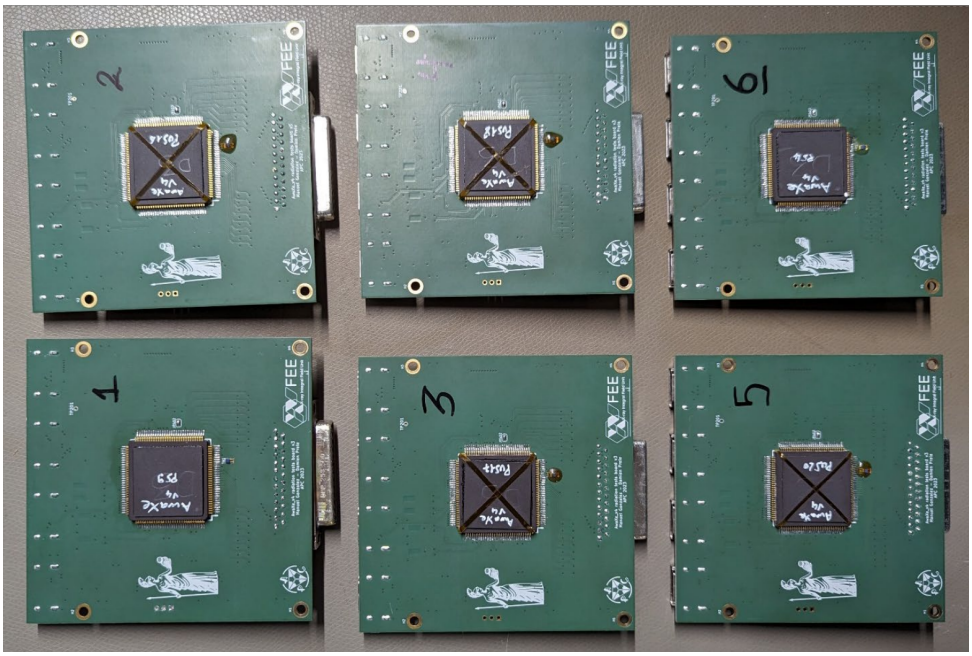

Figure 1: The ASIC boards used in the TID tests

This report present the data analysis of the total ionizing dose (TID) tests done on AwaXe_v4 ASIC. The ionizing tests were performed in October 2023 at the Fraunhoffer Institute in Euskirchen, Germany. The Fraunshoffer Institute TID report can be consulted in RD-03 . All irradiation and annealing steps were carried out in air. The samples were irradiated in ambient light at room temperature. The irradiation was carried out using the irradiation sources **TK100** and **TK1000B** of the institute.

The goal of the TID test is to characterize the variation of the parameters related to the total dose and to determine, where possible, the threshold where the performance of the components no longer meets the mission requirements. The TID test are divided into two main sets, one to study changes in the operating point of the internal electronic devices and the other to study the changes in noise due to the external radiation.

In order to test the AwaXe_v4 ASICs, six development boards were built. The development board schematics can be seen in RD-02. The sample boards are labeled 1 to 6 (see Figure 1). Five of the boards were irradiated and one was kept as reference (board number 6). The operating point measurements and noise measurements were performed on the six boards.

5 Test plan and data management

The test plan for irradiation is shown in Table 1. All the details of this test plan can be seen in the document AD-01. The test plan includes monitoring of the environmental temperature and recording of the power consumption of the devices when powered during an irradiation step.

The irradiation sequence was set in steps, resulting in a total of 7 steps to take into account for data analysis. Each step (except for steps 0 and 7) correspond to the total dose indicated in the first column of Table 1. There are measurements before starting the irradiation (*step 0*) and after each irradiation step. At the end of the irradiation process, a step of annealing[1] step (*step 7*) of one week

[1]See for reference Annealing (material science)

at 100 °C was performed for all the boards that were irradiated.

Total dose (krad)	Dose rate (krad/h)	Board 1		Board 2		Board 3		Board 4		Board 5		Board 6	
		Irr.	Bias	Irr.	Bias	Irr.	Bias	Irr.	Bias	Irr.	Bias	Irr.	Bias
6	0.036	✓	✗	✓	✗	✓	✗	✓	✓	✓	✗	✗	✗
12	0.036	✓	✓	✓	✓	✓	✓	✓	✓	✓	✗	✗	✗
18	0.036	✓	✓	✓	✓	✓	✓	✓	✓	✓	✗	✗	✗
36	0.360	✓	✓	✓	✓	✓	✓	✓	✓	✓	✗	✗	✗
100	36	✗	✗	✗	✗	✓	✓	✓	✓	✓	✗	✗	✗
200	36	✗	✗	✗	✗	✓	✓	✓	✓	✓	✗	✗	✗

Table 1: Dose test plan.

The Figure 2 shows the structure of the data provided by the Fraunhofer Institute personal after the irradiation test finished. The directory **B1500A** correspond to the operating point measurements performed with the Keysight B1500A Semiconductor Device Analyzer and the **Oszi** directory correspond to the LNAs and DACs noise measurements done with the Agilent 49410A Spectrum Analyzer.

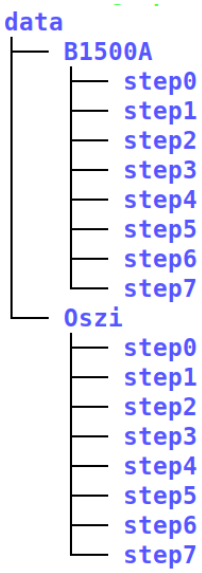

Figure 2: Test data tree.

The characterization of the ASIC internal components were performed with a Keysight B1500A Semiconductor Device Analyzer. Measurements were made following the expected total dose (in krad) as seen in the first column of Table 1 and following the Section 4 of the **AwaXe v4 TID testplan** document (AD-01). Figure 3 presents a block diagram of the AwaXe_v4 ASIC, showing the main components tested in Section 8.

This ASIC integrates two differential Low-Noise Amplifiers (LNA), two 8-bit slow Digital-to-Analog Converters (slowDAC) with different output ranges of current, a current reference (Iref) with four similar outputs, a thermometer, two identical PNP current mirrors accepting strong bias current of up to 10 mA and elementary components such as bipolar transistors (npnvhv, pnpl), MOSFETs (nmos25, pmos25), a capacitor (CMIM) and a resistor (Rpolysab). More details on the ASIC internals

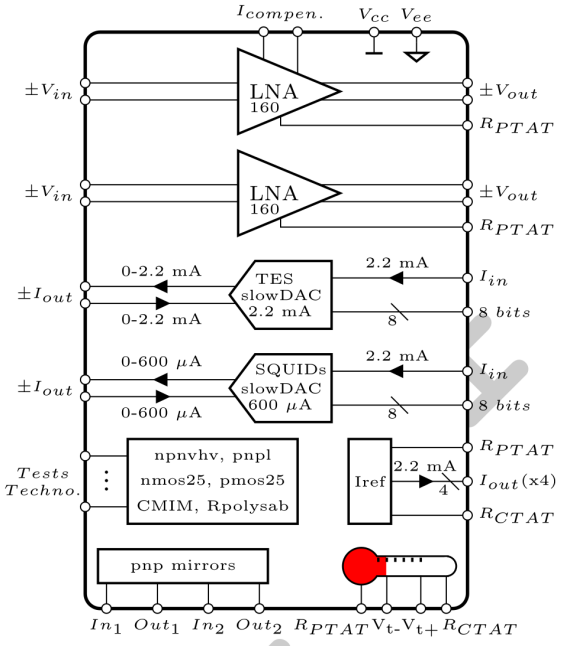

Figure 3: Block diagram of the AwaXe_v4 ASIC including all internal devices.

can be consulted in AwaXe_v4 datasheet (RD-01).

6 Test Support equipment

6.1 HDMI Board

An auxiliary board named "HDMI board" was built (see Figure 4 and RD-04) to be able to bias the test boards during the irradiation tests.

The HDMI board has basic biasing circuits for the internal active device in the AwaXe_v4 ASIC. The HDMI board provides the necessary power supply of 3.3 V arranged as: $V_{cc} = 1.65\,\text{V}$, $V_{ee} = -1.65\,\text{V}$ and $V_{cm} = 0\,\text{V}$ (1.65 V above V_{ee}).

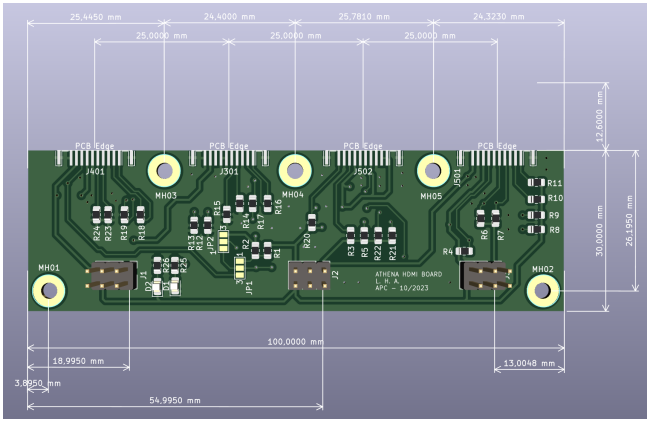

Figure 4: HDMI board used for biasing the ASIC boards during the irradiation tests.

7 Board status checks

All boards were verified after the irradiation process in terms of power consumption, capacitance of the MIM (Metal-Insulator-Metal) capacitor, gain of the LNAs and the correct functionality of the DACs. These measurements were done at the APC laboratory.

7.1 Power consumption

The power consumption of all the boards is analyzed in order to detect any damage or malfunction in the internal analog devices. Table 2 and Table 3 presents the results of the measurements done at APC after the TID tests, biasing the AwaXe_v4 boards through the HDMI board and without the HDMI board, respectively. The currents corresponds to the positive (I^+) and negative (I^-) lines of the power supply. These values coincides with the values reported in RD-03. Moreover, these values coincides with our own measurements done before all the irradiation process at APC.

Table 2 presents the power consumption of all internal components of the ASIC, including transistors (NMOS, PMOS, mirrors, etc.) and loaded LNA and DAC.

	V_{cc} [V]	I^+ [mA]	V_{ee} [V]	I^+ [mA]
Board 1	1.65	107	−1.66	−107
Board 2	1.65	101	−1.66	−101
Board 3	1.65	102	−1.66	−102
Board 4	1.65	101	−1.65	−101
Board 5	1.65	97	−1.65	−97
Board 6	1.65	101	−1.65	−101

Table 2: Power consumption of the AwaXe_v4 boards.

Table 3 shows the power consumption of the ASIC boards biasing only the LNA and DAC devices, and removing the HDMI board. As can be seen in Figure 5, these values are similar to the values reported in the RD-03. This results shows small or null changes in the power consumption of the boards between both measurements, indicating a good health of the LNA and DAC devices in the ASIC after the irradiation process. This hold true even for boards that have been exposed to the highest radiation doses.

	V_{cc} [V]	I^+ [mA]	V_{ee} [V]	I^+ [mA]
Board 1	1.65	90	−1.66	−90
Board 2	1.65	90	−1.66	−90
Board 3	1.65	85	−1.66	−85
Board 4	1.65	85	−1.65	−85
Board 5	1.65	84	−1.65	−84
Board 6	1.65	84	−1.65	−84

Table 3: Power consumption of the AwaXe_v4 boards biasing only the LNA and the DAC devices. For these measurements the HDMI board was removed.

7.2 LNA gain check

LNA device gain was measured for all the boards. Table 4 shows the measured values of the input (V_i) and output (V_o) voltages and the gain obtained as $G = \frac{V_o}{V_i}$.

Result 4: Bias Current

Bias Current	**[A]**							**AwaXe v4**
								WE: ---
K_{TL} with C=0.9, P=0.99, n=5: 4.666								
ON-Mode	**Co-60 Gammadose [krad(Si)]**							**Annealing**
Counter	**0**	**6**	**12**	**18**	**36**	**100**	**200**	**168 h 100°C**
B1	0.092	0.092	0.092	0.092	0.091			0.089
B2	0.092	0.092	0.089	0.088	0.090			0.087
B3	0.088	0.088	0.088	0.087	0.087	0.087	0.087	0.088
B4	0.088	0.084	0.087	0.088	0.087	0.086	0.086	0.087
B5	0.087	0.087	0.087	0.087	0.087	0.086	0.086	0.085
Radiation-Mean Off	**0.089**	**0.089**	**0.089**	**0.088**	**0.088**	**0.09**	**0.09**	**0.087**
Standarddeviation	**0.002**	**0.003**	**0.002**	**0.002**	**0.002**	**0.00**	**0.00**	**0.001**
K+	**0.101**	**0.105**	**0.098**	**0.098**	**0.097**	**0.089**	**0.089**	**0.094**
K-	**0.078**	**0.073**	**0.079**	**0.079**	**0.079**	**0.084**	**0.084**	**0.080**
Reference	**Co-60 Gammadose [krad(Si)]**							
Counter	**0**	**6**	**12**	**18**	**36**	**100**	**200**	**168 h 100°C**
B6	0.085	0.085	0.085	0.085	0.088	0.087	0.087	0.085

Figure 5: Bias current reported in the RD-03 document.

A maximum difference of 7 % was measured against the expected nominal gain of 80 V/V for this LNA configuration. There is no gain variation in the devices due to the irradiation process.

	V_i [mV]	V_o [mV]	Gain [V/V]	Diff %
Board 1	2.60	198.60	76.4	-4.5
Board 2	2.68	199.51	74.4	-7.0
Board 3	2.62	198.36	75.7	-5.3
Board 4	2.60	196.99	75.8	-5.2
Board 5	2.63	197.90	75.2	-6.0
Board 6	2.65	197.90	74.7	-6.6

Table 4: LNA input and output voltage measurements and gain calculus.

7.3 DAC output check

Table 5 presents the measurements of the output of the TES DAC devices (see Figure 3). These measurements corresponds to the voltage (V_o) over a $R = 510\,\Omega$ load resistor. The DACs were configured to output the mid-scale current level (FS/2)[2]. The percentage difference of the measured current against the nominal value expected for these devices is also presented.

An increase in the deviation of the output current was observed for boards 3, 4 and 5. These boards were exposed to the highest levels of total dose and dose rate. This effect may be related to some change in the current references of the DACs due to irradiation, but it is not clear which internal device is the most affected.

[2]FS: Full-scale

	V_o [mV]	I_o [mA]	Diff %
Board 1	-471	0.923	7.65
Board 2	-471	0.923	7.65
Board 3	-434	0.851	14.90
Board 4	-430	0.843	15.68
Board 5	-433	0.849	15.09
Board 6	-302	0.592	N/A

Table 5: Output voltage over a $R = 510\,\Omega$ load resistor for all DACs configured to operate at FS/2.

As can be seen in Table 5, the board 6 presents an anomaly in the TES DAC device, not related to the irradiation tests, as this board is used as control and was not irradiated. Because of this, the board 6 is excluded from the plots for the DACs performance analyses.

The TES DACs devices are affected by the irradiation process, which lowers the output current as the total dose increases. However, this effect is observed with a total dose level greater than the expected nominal mission level of 18 krad (Boards 1 and 2 were exposed to 36 krad and boards 3, 4 and 5 were exposed to 200 krad).

7.4 MIM capacitor value check

Table 6 presents the results of the capacitance measurements on the MIM capacitor in the ASIC. By design the capacitance of this device is $C_{MIM} = 150\,\text{pF}$ (see RD-01 and Section 8.14). The values correspond to three measurements: terminal A with respect to GND (C_A), terminal B with respect to GND (C_B) and between the capacitor's terminals (C_{AB}). The residual capacitance of the harness was also measured.

	C_A [pF]	C_B [pF]	C_{AB} [pF]
Harness Residual	140	120	40
Board 1	220	200	190
Board 2	220	200	190
Board 3	220	200	190
Board 4	200	190	190
Board 5	200	190	190
Board 6	200	190	200

Table 6: MIM capacitor measurements.

There are no changes in the capacitance of the C_{MIM} capacitor in the AwaXe_v4 devices due to the irradiation process.

7.5 LNA and DAC noise check

After the irradiation procedure, noise measurements were made on all boards to verify the status of the LNA and DAC devices. This extra step is identified as *step 8* and this section show the results obtained. The measurement setup is the same as that used for the dose tests and was performed in the low-noise APC room.

Noise measurements in LNA and DAC devices are presented in Figure 6 and Figure 7, respectively. The noise level is similar for all the devices and there are no observable effects over the voltage noise density of these devices due to the total dose tests.

As was mentioned before, board 6 presents an anomaly in the TES DAC device and is excluded from the plots for the DACs performance analyses.

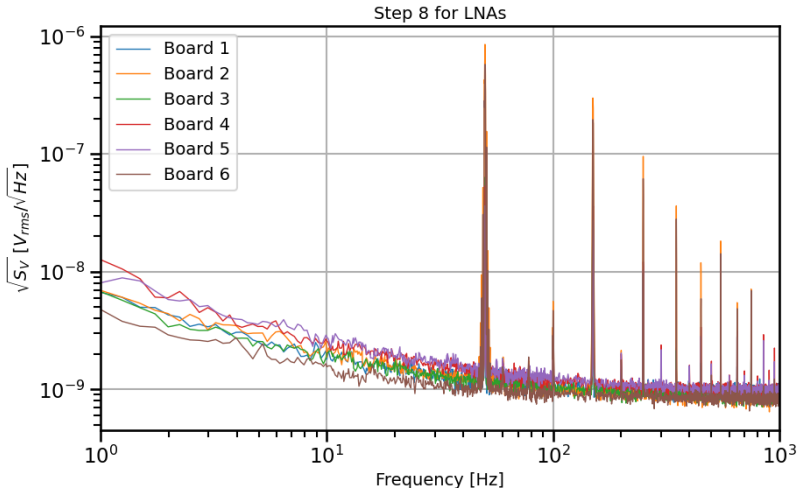

Figure 6: LNA noise measurements at APC (*step 8*).

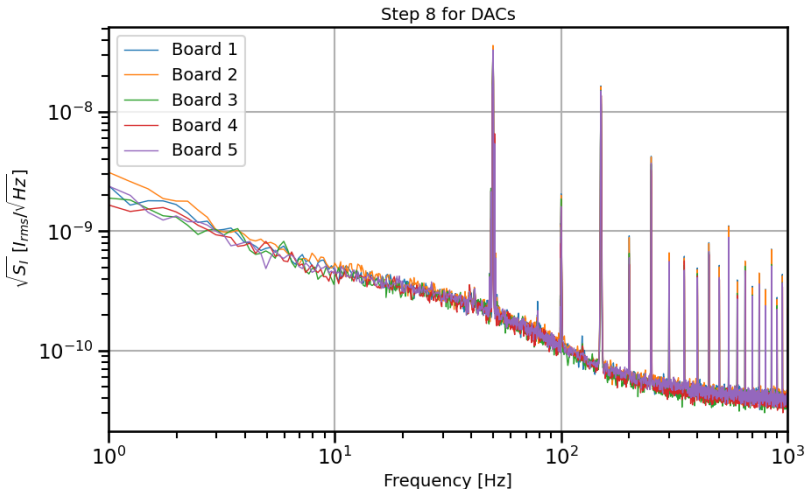

Figure 7: DAC noise measurements at APC (*step 8*).

8 Semiconductor individual components tests

Individual component tests are presented in this section. The characterizations were performed using a Keysight B1500A Semiconductor Device Analyzer.

The HDMI board was used to bias all the transistors to obtain a biasing current of 1 mA for reference. The LNAs are polarized using two 50 Ω resistors to ground at the input and a 100 Ω resistor at the output in order to obtain a nominal impedance adaptation. In addition, there are a 100 Ω load resistor in the SQUID DAC output and a 40 Ω load resistor in the TES DAC output.

The results presented correspond to measurements of the active devices in a low-current regime. This regime is convenient because it will allow us to observe the effects of the irradiation in the internal devices of the ASIC (otherwise, these effects could be difficult to appreciate in the nominal regime of these devices).

In the following sections are presented the plots of the data from board 3 compared to board 6 (taken as reference). The board 3 was selected as this board was irradiated in all the irradiation steps and biased almost all the time, except for *step 1*. The data plots of board 3 are representative of the

responses of the other boards, and, in general, the responses due the irradiation process are similar for the rest of the boards. For reference, the plots of all the board are available in the Appendix A.

8.1 Current Mirror

This measurement corresponds to the variation of the operating point in the irradiation process of the PNP mirrors inside the AwaXe_v4 ASIC. Figure 8 shows the electronic schematic of these two identical PNP current mirrors capable of accepting strong bias current (up to 10 mA) and aiming to change the current direction of the DAC present in the Digital Readout Electronics (DRE).

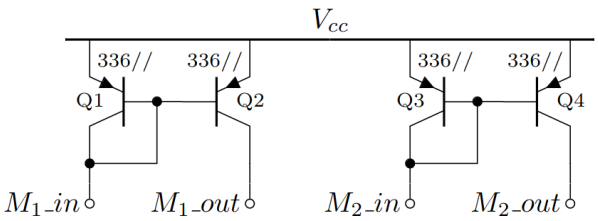

Figure 8: Two PNP current mirrors within the ASIC.

The parameter M shown in Figure 9 corresponds to the ratio I_{out}/I_{in} over the current mirror, where I_{in} is the input current and I_{out} is the output current of the mirror. The figure presents output (mI_M_OUT) versus the input (mI_M_IN) current and the $M = I_{out}/I_{in}$ parameter versus the input current. It is also included the *step 0*, before the irradiation, and *step 7* (Ann) corresponding to the measurements made after the annealing process. It is expected to have a value $M = 1$ under nominal conditions for these devices.

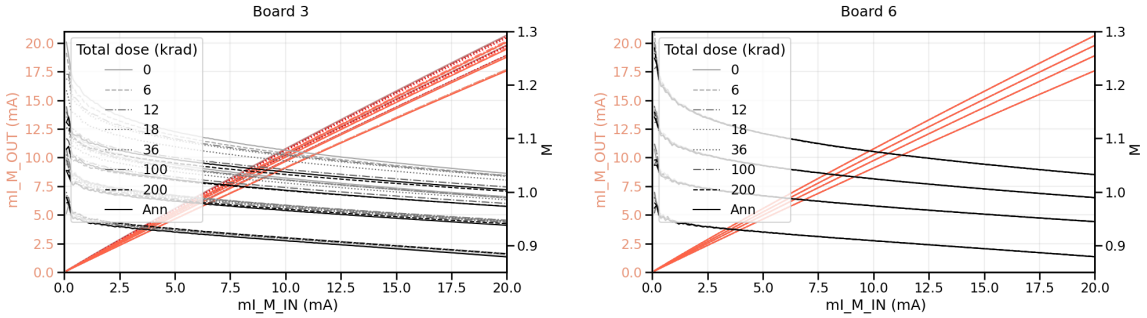

Figure 9: Characterization of the PNP current mirror. Results of board 3 (left) compared to the results of the characterization of board 6 as a reference (right).

Based on the plots shown in Figure 9, it can be seen a change of ∼5% in the parameter M in the higher-current valued curves and, in general, it is possible to say the changes are not reversible, marked by the curve Ann (black solid lines) in the plots. In the lower-current-valued curves, it can be seen even less change, ∼1% compared to the previous. The measurements for the six boards can be seen in the Appendix A.1.

8.2 NPN1 GP

The ASIC has a pair of integrated NPN (NPN1 and NPN2) high-voltage Heterojunction Bipolar Transistors (HBT) for DC and rad-hard characterization. Each NPN transistor is composed of 8 parallel transistors with 5 emitters, 10 bases, and 6 collectors having the same dimensions as the

ones used in the LNA. The 16 transistors also form a 4×4 common-centroid pattern, the same as a differential pair in the LNA.

The Gummel plot for the NPN1 transistor is presented in Figure 10. The β parameter of the transistor is affected by dose. This parameter shows a change of the order of ∼55% going down in value, being one of the most affected parameters in all measurements. However, after the annealing process there is a small recovering, reaching a ∼40% of the original value.

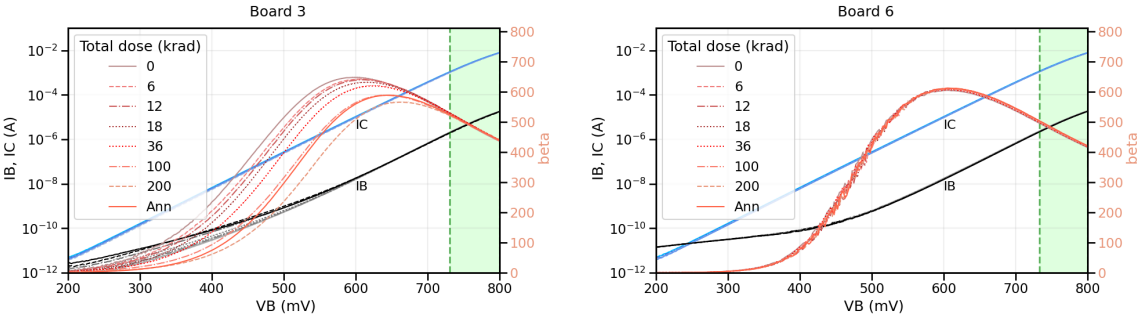

Figure 10: Gummel plots of the NPN1 device in the ASIC. Results for board 3 (left) compared to board 6 (right).

The green shaded region in the plots in Figure 10 indicates the intended operation zone in nominal conditions. The radiation effects can be neglected. The measurements for the six boards can be seen in the Appendix A.2.

8.3 NPN1 IC VCE

The characteristic curve of the NPN1 transistor show no changes along the radiation process, as can bee seen in Figure 11. There are no significant changes to mention. The measurements for the six boards can be seen in the Appendix A.3.

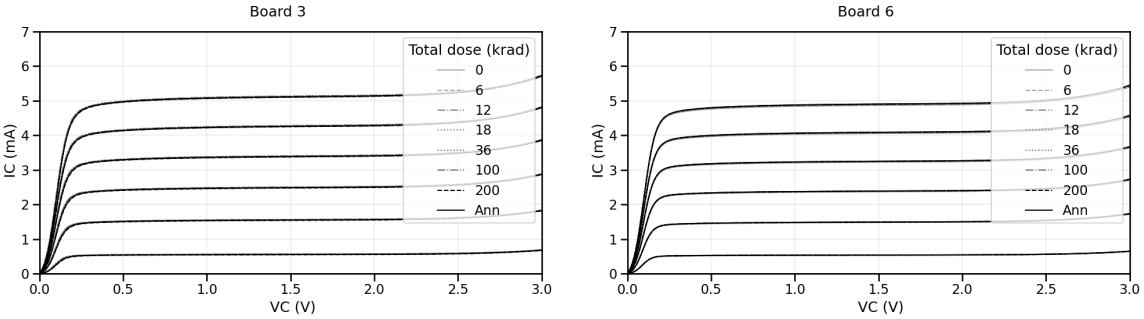

Figure 11: Characteristic curve of the NPN1 transistor. Results for board 3 (left) compared to board 6 (right).

8.4 NPN2 GP

The results for this device, presented in Figure 12, are similar to those of the NPN1 device analyzed in section 8.2. The green shaded region in the plots indicates the intended operation zone in nominal conditions. The radiation effects can be neglected. The measurements for the six boards can be seen in the Appendix A.4.

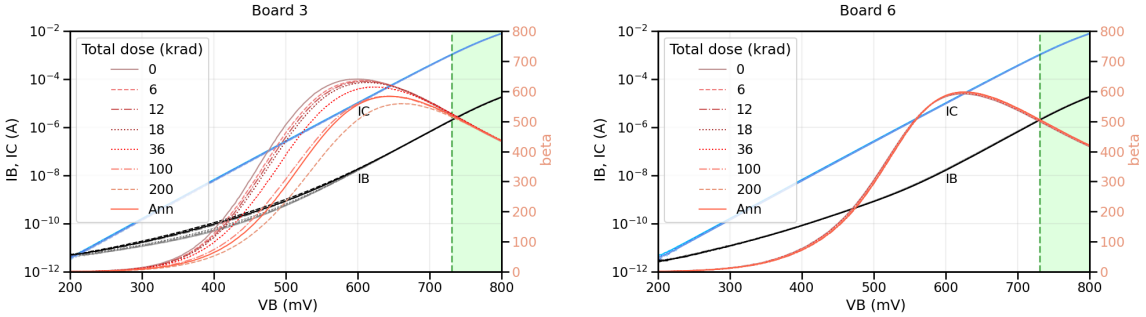

Figure 12: Gummel plots of the NPN2 device in the ASIC. Results from board 3 (left) compared to board 6 (right).

8.5 NPN2 IC VCE

The results for this device, presented in Figure 13, are similar to those for the NPN1 device in section 8.3. There are no changes to mention due to the irradiation process. The measurements for the six boards can be seen in the Appendix A.5.

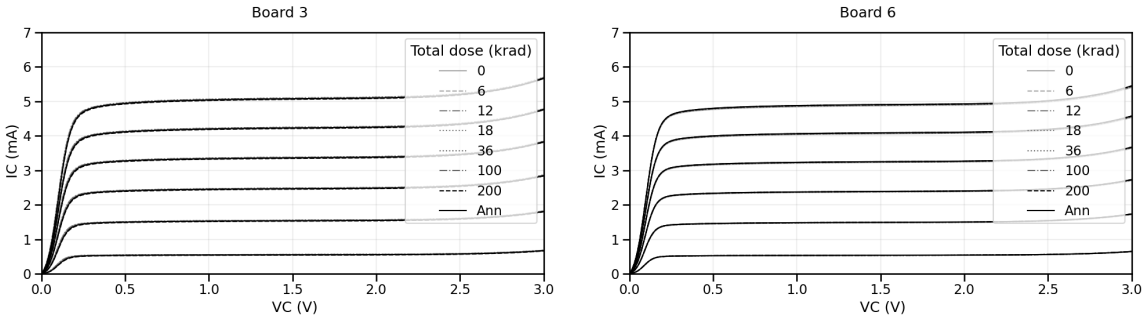

Figure 13: Characteristic curve of the NPN2 transistor. Results for board 3 (left) compared to board 6 (right).

8.6 PNP GP

The ASIC has an integrated PNP lateral bipolar transistor for DC and rad-hard characterization. The dimension of this type of transistor is unchangeable, with single emitter of $1.2\,\mu\text{m} \times 1.2\,\mu\text{m}$. This transistor is composed of 336 parallel transistors of default dimension, the same number used in the LNA first active load. The total surface of the emitter is $1.2\,\mu\text{m} \times 1.2\,\mu\text{m} \times 336 = 483.84\,\mu\text{m}$ (RD-01). The Gummel plot for this transistor is presented in Figure 14. The measurements for the six boards can be seen in the Appendix A.6.

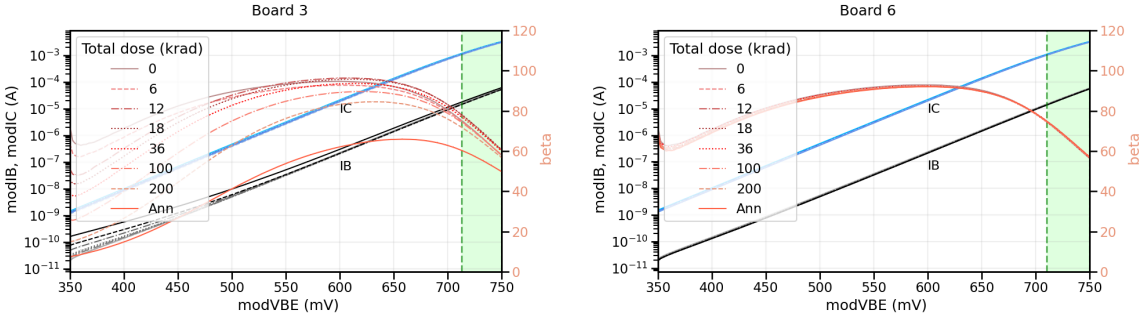

Figure 14: Gummel plots of the PNP device in the ASIC. Results for board 3 (left) compared to board 6 (right).

As the NPN transistors, the PNP transistor also suffers a change in the parameter β. This change is of the order of ∼33% less compared to the initial value, going down in value as the total dose increase, being one of the most affected parameters in all the measurements for all the boards. In this case, as opposed to what happened in the NPN transistors, after the annealing process there is no recovering. Even, the β value moves further away from the original value.

The green shaded region in the plots in Figure 14 indicates the intended operation zone in nominal conditions. The radiation effects have an important impact over the β parameter for the PNP transistor.

8.7 PNP IC VCE

The characteristic curves of the ASIC's PNP transistor are presented in Figure 15. This device, unlike NPN transistors, has a current change of ∼6.7% for the higher current values in the characteristic curve. Similar to the β parameter after the annealing process, the PNP transistors are not recovering the original values, maintaining a final difference of ∼16.7% against the original current values. The measurements for the six boards can be seen in the Appendix A.7.

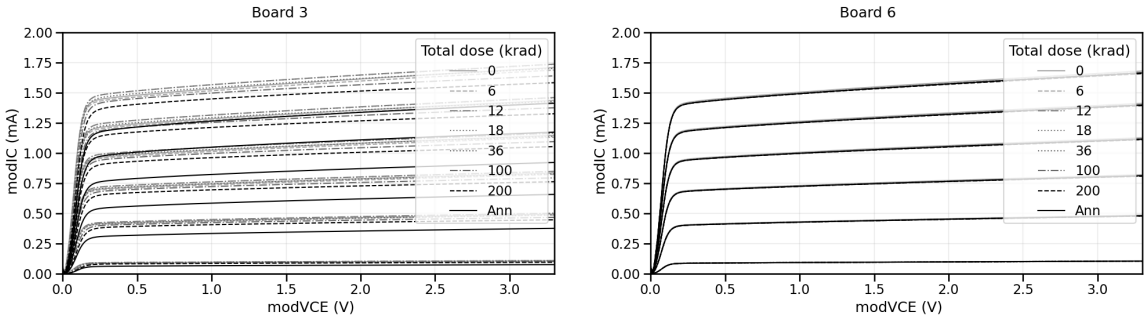

Figure 15: Characteristic curve of the PNP transistor. Results for board 3 (left) compared to board 6 (right).

8.8 NMOS1 ID VGS

The ASIC has two integrated high-voltage NMOS transistors for DC and rad-hard characterization. They can also serve as a pair of differential switches, with the sources as inputs and the drains as outputs. The gates are connected together to open/close the switches, as shown in Figure 16. The switches are planned to be connected at the LNA inputs to isolate that device from strong currents if necessary.

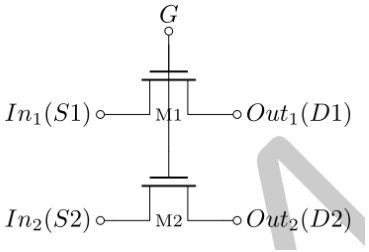

Figure 16: Simplified schematic of the NMOS switches present in the AwaXe_v4 ASIC.

In Figure 17 there are no observable effects on the NMOS1 device after the irradiation process. The measurements for the six boards can be seen in the Appendix A.8.

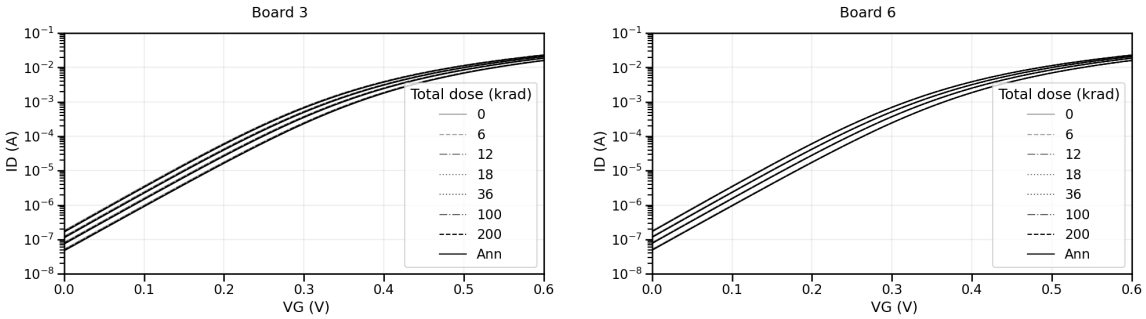

Figure 17: Characteristic curves for the NMOS1 transistor. Results for board 3 (left) compared to board 6 (right).

8.9 NMOS1 ID VDS

In Figure 18 there are no observable effects on the NMOS1 device after the irradiation process. The measurements for the six boards can be seen in the Appendix A.9.

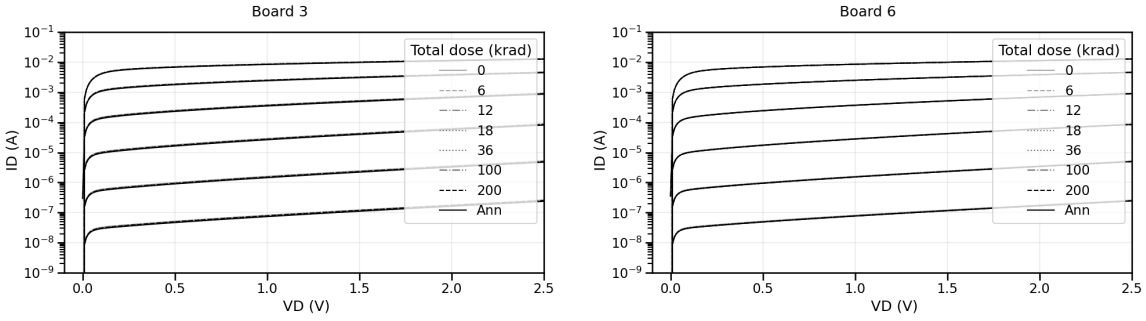

Figure 18: Characteristic curves for the NMOS1 transistor. Results for board 3 (left) compared to board 6 (right).

8.10 NMOS2 ID VGS

In Figure 19 there are no observable effects on the NMOS2 device after the irradiation process. The measurements for the six boards can be seen in the Appendix A.10.

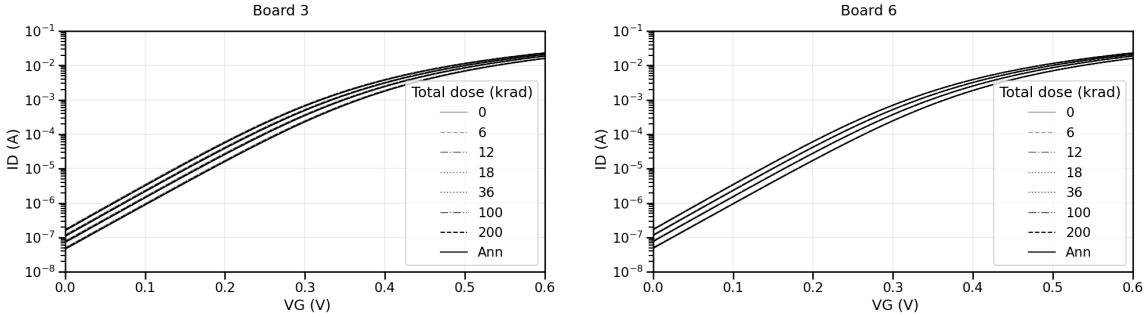

Figure 19: Characteristic curves for the NMOS2 transistor. Results for board 3 (left) compared to board 6 (right).

8.11 NMOS2 ID VDS

In Figure 20 there are no observable effects on the NMOS2 device after the irradiation process. The measurements for the six boards can be seen in the Appendix A.11.

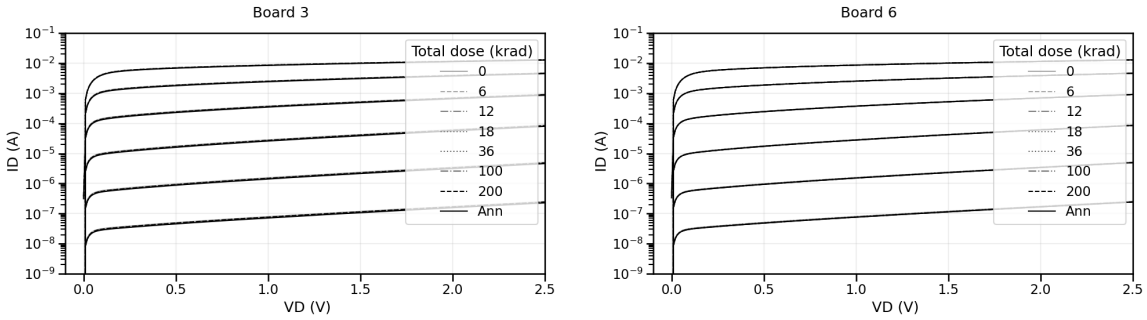

Figure 20: Characteristic curves for the NMOS2 transistor. Results for board 3 (left) compared to board 6 (right).

8.12 PMOS ID VGS

The ASIC has an integrated high-voltage PMOS transistor for DC and rad-hard characterization. In Figure 21 there are no observable effects on the PMOS device after the irradiation process. The measurements for the six boards can be seen in the Appendix A.12.

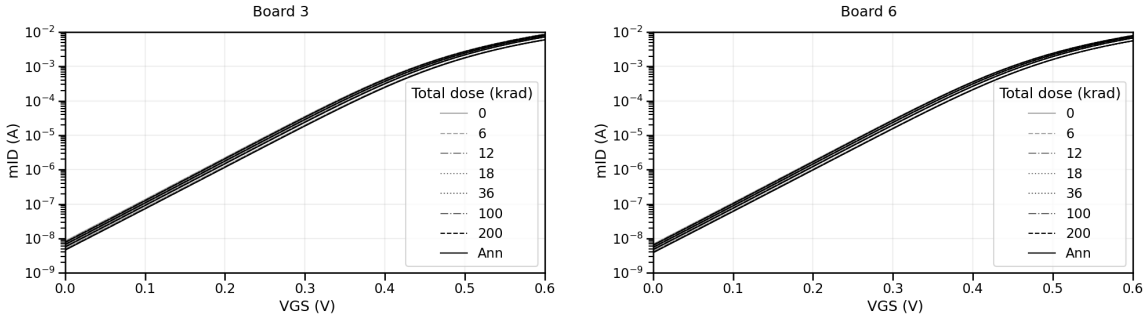

Figure 21: Characteristic curves for the PMOS transistor. Results for board 3 (left) compared to board 6 (right).

8.13 PMOS ID VDS

In Figure 22 there are no observable effects on the PMOS device after the irradiation process. The measurements for the six boards can be seen in the Appendix A.13.

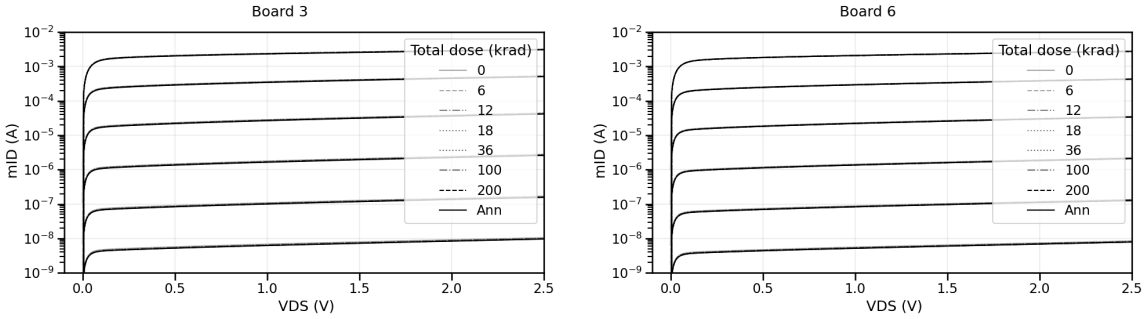

Figure 22: Characteristic curves for the PMOS transistor. Results for board 3 (left) compared to board 6 (right).

8.14 Capacitor leakage

The ST 130 nm SiGe BiCMOS technology offers MIM capacitors that are not possible to have with the AMS 350 nm SiGe BiCMOS technology. The capacitor uses layers that are on top of the 6 metal layers, saving space compared to poly capacitors. The AwaXe_v4 ASIC has massively integrated MIM capacitors to be used as start-up reference and as decoupling between V_{cc} and V_{ee}. The ASIC has a 150 pF capacitor (conformed by six 25 pF capacitors in parallel) as a component to be characterized. One of the main radiation problems with capacitors is the increase of current leakage. The measurements for current leakages are presented in Figure 23. The measurements for the six boards can be seen in the Appendix A.14.

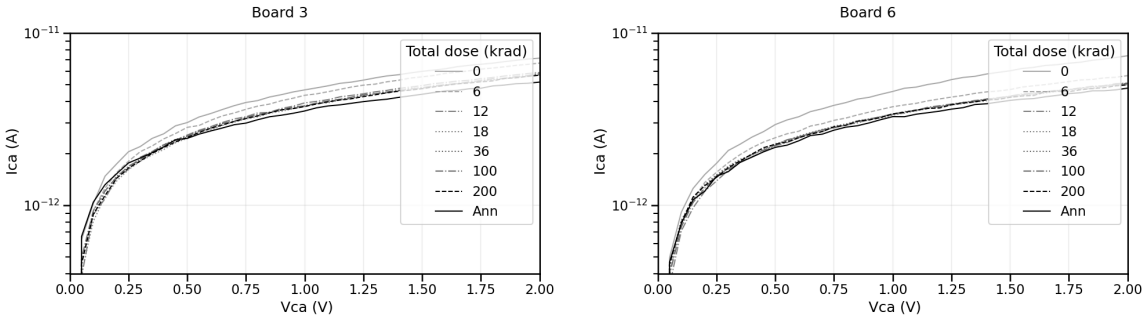

Figure 23: Leakage current due to in-chip MIM capacitor. Results for board 3 (left) compared to board 6 (right).

An increase of the leakage was expected, but a small decrease was measured. This is compatible with a residual leakage in the PCB due to humidity or flux, which was cured with time. There are not increase of current leakage observed as conclusion.

9 LNA and DAC noise measurements

One important characteristic of the AwaXe_v4 device is the noise behavior. In this section is presented the irradiation impact on the LNA noise and DAC noise. The goal of this measurements is

to find the values of the intrinsic input voltage noise source e_n (for the LNA) and the intrinsic output current noise source i_n (for the DAC).

The noise measurements were performed after each irradiation step in all the boards. The frequency range of interest is from 1 Hz to 1000 Hz. This range of frequencies is divided into two regions, one low-frequency (LF) region from 1 Hz to 100 Hz and a high-frequency (HF) region from 10 Hz up to 1000 Hz. This allows to have an overlap within the range of 10 to 100 Hz to verify the homogeneity of the measurement. For each experiment (LNA or DAC) there will be two measurements, corresponding to the LF and HF regions, respectively.

The experimental setup for the measurement of the noise characteristics of both devices was the same. A Keysight E3649A power supply was used to bias the boards (differential voltage V_{cc} and V_{ee}). The output data was amplified by a Stanford Research SR650 low-noise amplifier (two SR650 instruments were used, one for the LNA and one for the DAC), and for visualization and record, an Agilent 89410A Vector Signal Analyzer was used. The setup and procedures are available in AD-01.

In order to understand how to analyze the data from the noise measurements, the noise path is presented in Figure 24 for the LNA and Figure 25 for the DAC.

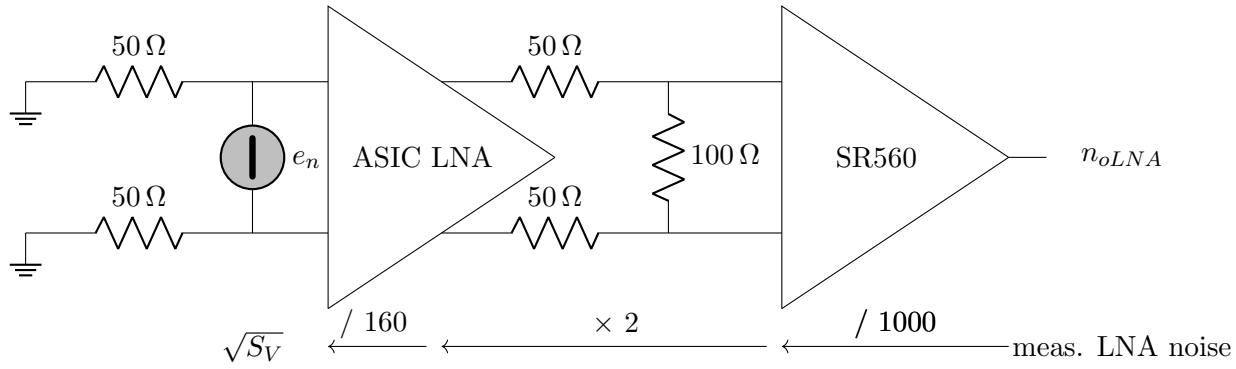

Figure 24: Electronic schematic showing the LNA noise measurement setup.

For the LNA noise measurements the input noise density, $\sqrt{S_V}$, for the value of the gain $G = 160\,\mathrm{V/V}$ of the LNA and the value of the the Stanford Research amplifier gain $G = 1000$, the value of the input noise source, can be calculated with the equation:

$$n_{oLNA} = \frac{G_{LNA} \cdot G_{SRA} \cdot \sqrt{S_V}}{2} \Rightarrow \sqrt{S_V} = \frac{n_{oLNA}}{80000} \quad [V/\sqrt{Hz}] \tag{1}$$

The input noise density is the combination of the intrinsic LNA voltage noise e_n, the thermal noise due to the input resistors ($R_{in} = 50\,\Omega + 50\,\Omega = 100\,\Omega$ in differential) and the noise of the Stanford Research amplifier, $e_{nSR1} = 3.5\,\mathrm{nV}/\sqrt{Hz}$ @ 1 kHz, then

$$\sqrt{S_V} = \sqrt{e_n^2 + 4 \cdot k_B \cdot T \cdot R_{in} + \left(\frac{e_{nSR1}}{80}\right)^2} = \frac{n_{oLNA}}{80000} \tag{2}$$

Using the previous equations, solving for e_n:

$$e_n = \sqrt{\left(\frac{n_{oLNA}}{80000}\right)^2 - 4 \cdot k_B \cdot T \cdot R_{in} - \left(\frac{e_{nSR1}}{80}\right)^2} \quad [V/\sqrt{Hz}] \tag{3}$$

For the previous equation T is the room temperature (300 K) and k_B is the Boltzmann constant ($k_B = 1.38 \times 10^{-23} J/K$).

The noise term related to the Stanford Research amplifier, e_{nSR1}, is comparatively negligible with the other two terms and can be removed:

$$e_n = \sqrt{\left(\frac{n_{oLNA}}{80000}\right)^2 - 4 \cdot k_B \cdot T \cdot R_{in}} \quad [V/\sqrt{Hz}] \tag{4}$$

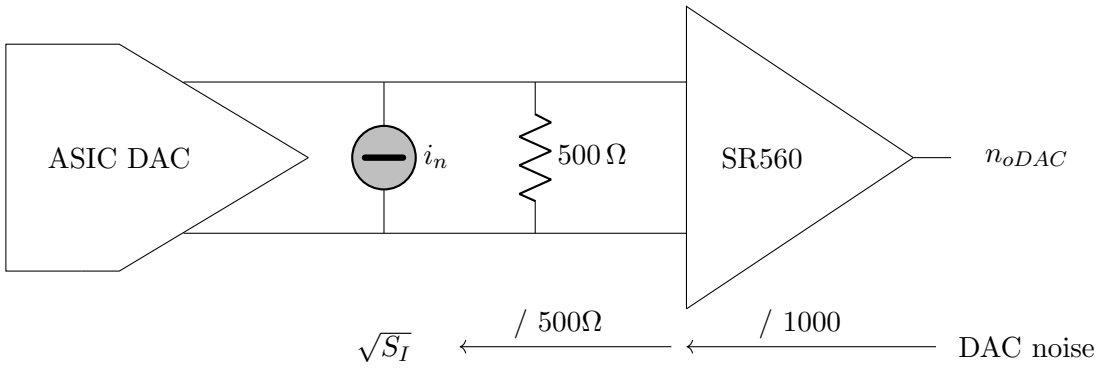

Figure 25: Electronic schematic showing the DAC noise measurement setup.

For the noise measurement of the DAC, a load resistor $R_o = 500\,\Omega$ is used to convert it to voltage noise and a gain $G = 1000$ of the Stanford Research amplifier (see Figure 25) has to be considered, resulting in the following equation:

$$n_{oDAC} = G \cdot R_o \cdot \sqrt{S_I} = 1000 \cdot 500 \cdot \sqrt{S_I} \Rightarrow \sqrt{S_I} = \frac{n_{oDAC}}{500000} \quad [A/\sqrt{Hz}] \tag{5}$$

The DAC output density noise is the combination of the intrinsic current noise i_n, the thermal noise due to the resistance R_o and the noise added by the Stanford Research amplifier ($e_{nSR2} = 5\,\mathrm{nV}/\sqrt{Hz}\,@\,1\,\mathrm{kHz}$) resulting in the equation:

$$\sqrt{S_I} = \sqrt{i_n^2 + \frac{4 \cdot k_B \cdot T}{500} + \left(\frac{e_{nSR2}}{500}\right)^2} \tag{6}$$

Using the previous equations, solving for i_n:

$$i_n = \sqrt{\left(\frac{n_{oDAC}}{500000}\right)^2 - \frac{4 \cdot k_B \cdot T}{500} - \left(\frac{5 \times 10^{-9}}{500}\right)^2} \quad [A/\sqrt{Hz}] \tag{7}$$

9.1 Data cleaning and analysis

Before we perform the data analysis of the noise measurements from the irradiation procedure it was necessary to review and clean the dataset. Giving a first view to the data we observe some no-homogeneity and some jumps in sections of the dataset. We attribute these no-homogeneity in the data to the fact that these measurements were not performed in a low-noise room and also to some mistakes in the data taking process (incorrect waiting time for the time constant setup in the spectrum analyzer, some imperfect cable connections, etc.)

In the following sections the results of noise measurement are presented. In this sectionthe boards 2, 3 and 5 are chosen for their stability and homogeneity of the measured data. One important point to be noted is that board 1 and 2 where turned off and no longer receive irradiation after the *step 3*, so there are no data in *steps 5* and *6* for these boards.

9.2 DAC noise measurement

The current noise density plot of the DAC devices in boards 2 and 5 is presented in Figure 26. These plots show how even in the same board there are data that is not homogeneous in some steps. The dataset was filtered in order to maintain only data with some physical meaning.

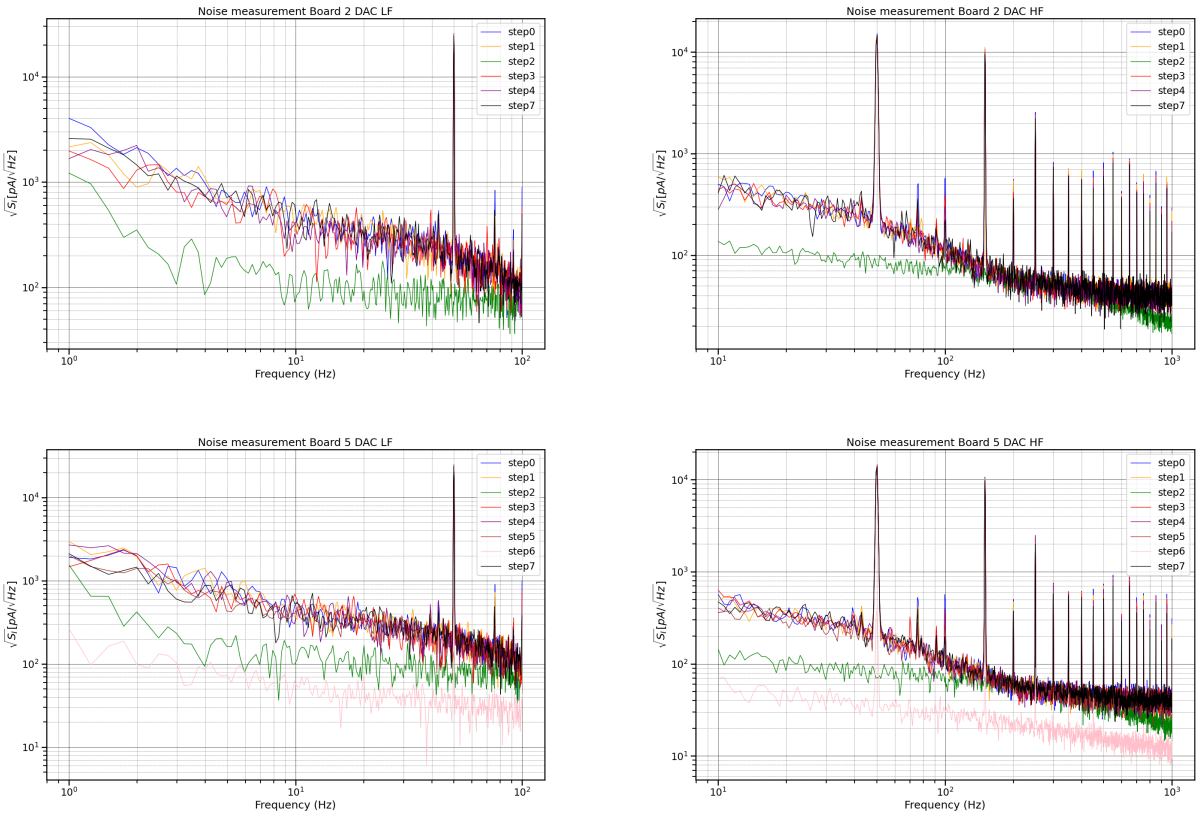

Figure 26: Current noise density ($\sqrt{S_I}$) for the DAC of boards 2 and 5 in the low frequency (left) and high frequency (right) ranges.

Analyzing the Figure 26, a decrease of the noise amplitude can be observed in *step 2* in the low-frequency plots ($1 - 100$ Hz). The *step 2* corresponds to the total dose level of 12 krad, so there is no physical reason of this amplitude drop during this step. This event happens in all the boards at *step 2* for DAC noise measurement, meaning that this data can be filtered from the dataset. The measurement in board 5 also shows that the noise amplitude decreases in *step 6*, corresponding to the total dose level of 200 krad. Observing the plots of board 5 at *step 7* (turn off the irradiation and annealing for one week) the noise amplitude is significantly higher than at *step 6*. The event happen only in board 5, so we consider removing it from the dataset to be analyzed in this report and consider a deeper analysis in the future. While investigating the DAC noise dataset, some data was removed from the dataset due to the no-homogeneity between themselves and other boards, some other due to the discontinuity between LF and HF. All the DAC plots for all the steps is presented in the Appendix B for reference.

9.3 LNA noise measurement

Figure 27 presents the plot of the voltage noise density of the LNA devices in boards 2 and 5. These plots show how even in the same board there are data that is not homogeneous in some steps. The dataset has been filtered in order to maintain only the ones having some physical meaning.

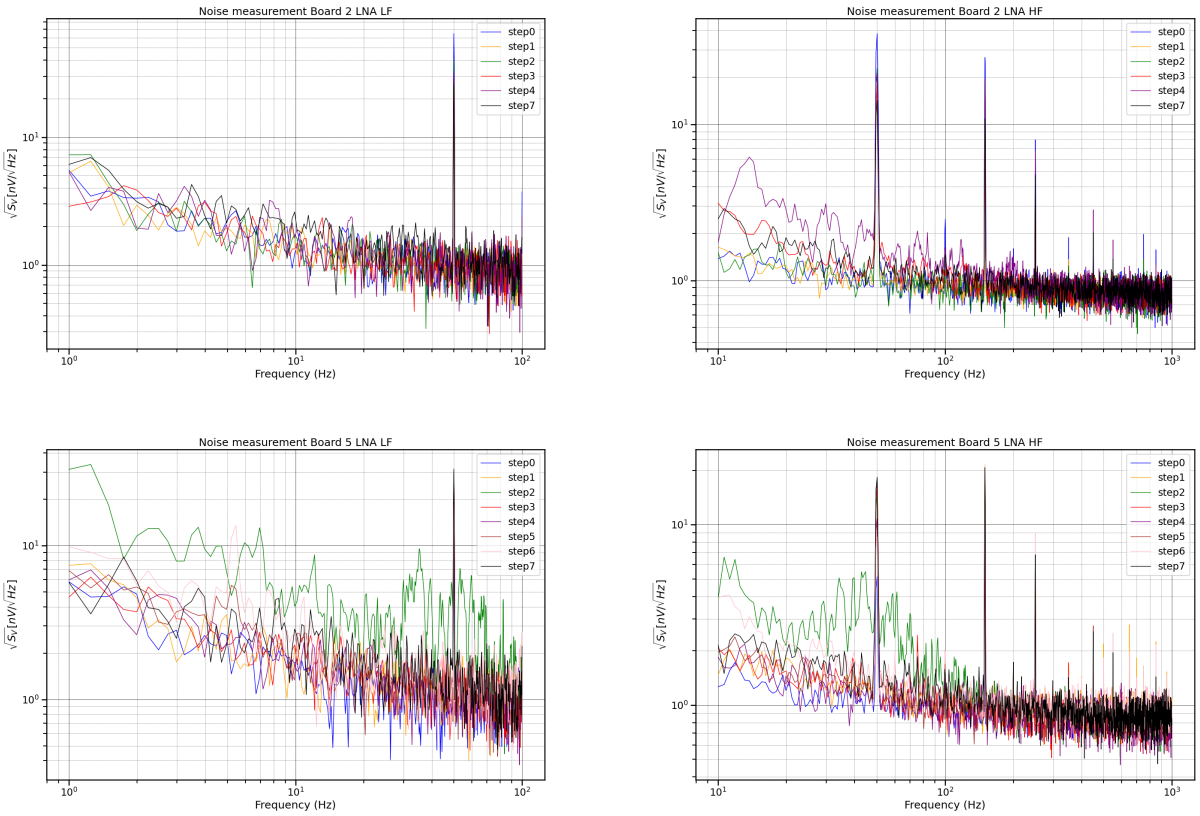

Figure 27: Voltage noise density ($\sqrt{S_V}$) for the LNA of boards 2 and 5 in the low frequency (left) and high frequency (right) ranges.

The results obtained from the LNA noise measurements are more stable, being more homogeneous between the LF and HF ranges, than those of the DACs. However, with the board 3, there is an anomalous behavior specifically during *step 2* (see the Appendix B). The same occurrence is observed in some boards, but not consistently across all boards. Therefore, these anomalous data are excluded from the analysis. Additionally, certain data during *steps 3*, *5*, *6*, and *7* in some boards exhibit unique behaviors that are not consistently present across all boards and does not correspond to any expected physical behavior of this electronic devices. Consequently, these specific data points are removed from the analysis.

9.4 White noise analysis

Assuming a Gaussian distribution of the white noise portion of the data, a Shapiro-Wilk test[3] was performed over the dataset with the significant level $\alpha = 0.05$ along the high frequency part of the HF range of the measurements ($300 - 1000$ Hz). Table 7 shows the results of the Shapiro-Wilk test applied to the white noise analysis.

[3]Biometrika, Volume 52, Issue 3-4, December 1965, Pages 591–611, https://doi.org/10.1093/biomet/52.3-4.591

Step	**Board number**	**White noise** ($\mu \pm \sigma$)	
		DAC (**pA**/$\sqrt{Hz}$)	**LNA** (**nV**/$\sqrt{Hz}$)
Step 0	Board 1	44 ± 7	0.9 ± 0.1
	Board 2	41 ± 5	0.8 ± 0.1
	Board 3	42 ± 6	0.8 ± 0.1
	Board 4	42 ± 6	1.1 ± 0.2
	Board 5	41 ± 7	0.9 ± 0.1
	Board 6	41 ± 6	0.8 ± 0.1
Step 1	Board 1	43 ± 6	0.9 ± 0.1
	Board 2	44 ± 6	0.9 ± 0.1
	Board 3	42 ± 5	0.8 ± 0.1
	Board 4	45 ± 7	0.9 ± 0.1
	Board 5	43 ± 6	0.9 ± 0.1
	Board 6	41 ± 6	0.8 ± 0.1
Step 2	Board 1		0.9 ± 0.1
	Board 2		0.8 ± 0.1
	Board 3		0.8 ± 0.1
	Board 4		
	Board 5		
	Board 6		0.9 ± 0.1
Step 3	Board 1	63 ± 9	
	Board 2	41 ± 5	
	Board 3	62 ± 10	0.9 ± 0.1
	Board 4	58 ± 7	0.9 ± 0.1
	Board 5	43 ± 6	
	Board 6		
Step 4	Board 1	50 ± 7	
	Board 2	41 ± 6	
	Board 3	46 ± 7	0.8 ± 0.1
	Board 4	47 ± 6	0.9 ± 0.1
	Board 5	41 ± 6	0.8 ± 0.1
	Board 6		0.8 ± 0.1
Step 5	Board 1		
	Board 2		
	Board 3	40 ± 5	0.9 ± 0.1
	Board 4	39 ± 5	1.1 ± 0.1
	Board 5	39 ± 6	0.9 ± 0.1
	Board 6		
Step 6	Board 1		
	Board 2		
	Board 3	39 ± 7	1.0 ± 0.1
	Board 4	40 ± 6	1.4 ± 0.2
	Board 5		0.9 ± 0.1
	Board 6		0.9 ± 0.1
Step 7	Board 1	95 ± 20	
	Board 2	41 ± 8	0.9 ± 0.1
	Board 3	45 ± 8	0.9 ± 0.1
	Board 4	44 ± 6	
	Board 5	41 ± 6	0.9 ± 0.1
	Board 6		

Table 7: Parameter extraction of the white noise region of the dataset.

Figure 28 shows a plot of the DAC parameter extraction presented in Table 7. The DACs have an average white noise density of $43 \pm 7\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$.

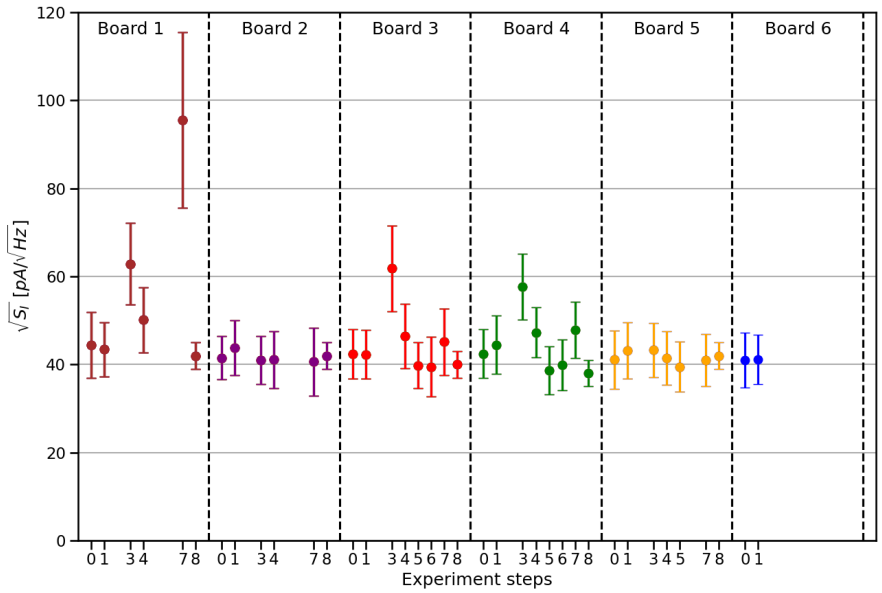

Figure 28: Current noise density of the DACs in the analyzed white noise region ($300 - 1000\,\mathrm{Hz}$).

Figure 29 shows a plot of the LNA parameter extraction presented in Table 7. The LNAs have an average white noise density of $0.9 \pm 0.1\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$.

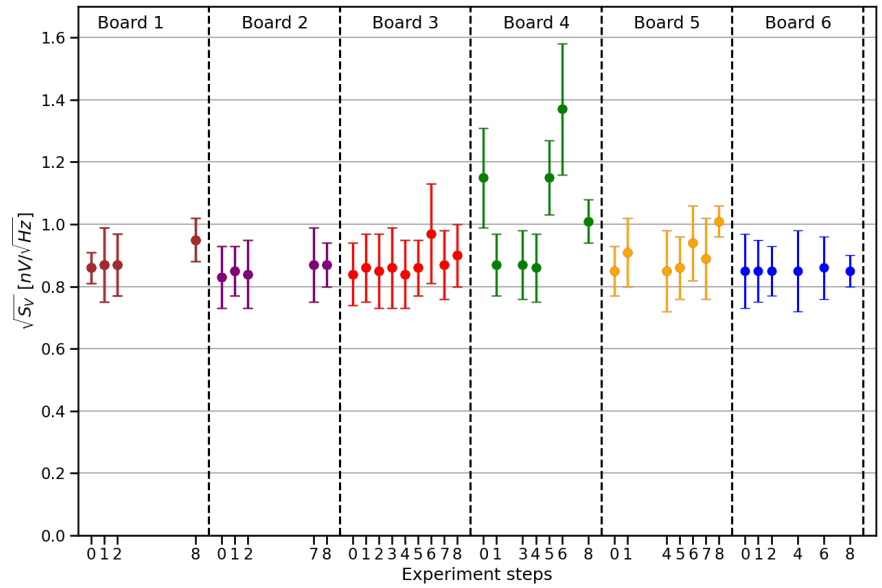

Figure 29: Voltage noise density of the LNAs in the analyzed white noise region ($300 - 1000\,\mathrm{Hz}$).

9.5 Corner frequency analysis

A curve fitting algorithm was applied over the density curves obtained during the irradiation steps, with the next considerations:

1. The data set is filtered for the frequency peak of the AC line and its harmonics (50 Hz, 100 Hz, 150 Hz). These peaks can bias the dataset and lead to failure of the curve fitting algorithm. Appendix B shows plots of the complete noise dataset.

2. The frequency ranges LF and HF are merged to a final total frequency range from 1 Hz to 1000 Hz.

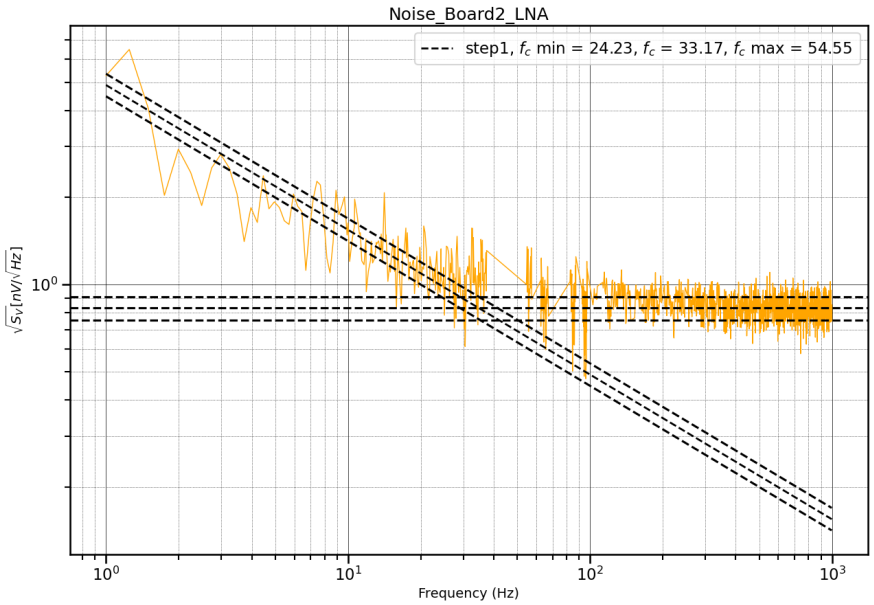

Figure 30: Corner frequency finding method applied to the board 2 in *step 1*.

The corner frequency are defined as the intersection between the flicker noise ($1/f$) and the white noise regions. By applying the fit separately in the flicker noise and white noise regions, the value of the corner frequency can be found. In order to add a figure of merit to the method, a range of corner frequency obtained as the intersection of its standard deviations is included. Figure 30 is an example showing this method, applied to the noise density of board 2 in *step 1*.

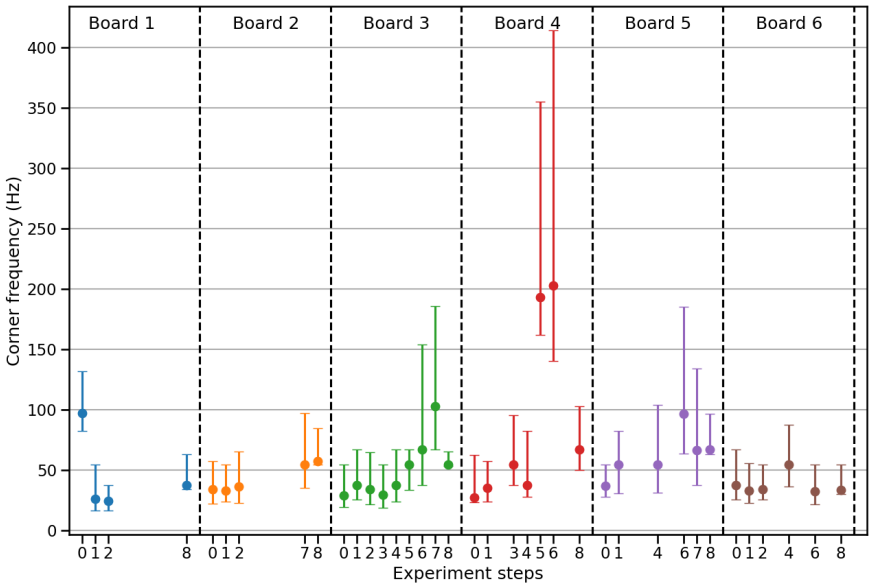

Figure 31: Corner frequencies for all the boards found applying the finding method. Error bar plot are used to visualize the data presented in Table 8. Bullet symbols represent the mean white noise value, while the upper and lower sticks represent the error of the finding method.

From Figure 31 it can be seen that the corner frequency obtained by the fitting method vary from 20 Hz to a maximum value of more than 400 Hz (board 4, *step 6*). The large variation could come from the imperfect filtering of the data, as the data filtering was applied globally and there are some boards noisier than others. Most of the calculated corner frequencies are distributed in the range from 20 Hz to 80 Hz.

The Table 8 summarizes the data obtained for the corner frequency finding.

For this section only the LNA data analysis is presented as it can be modeled as the simple intersection of two curves. The DAC data presents a different shape in the flicker noise region (see Appendix B). This region can not be analyzed by a simple model as done with the LNA data and requires a more elaborated model to take into account all the system noise contributions.

Step	Board	Corner frequency (Hz)
Step 0	Board 1	97^{+35}_{-15}
	Board 2	34^{+23}_{-12}
	Board 3	29^{+26}_{-9}
	Board 4	27^{+35}_{-4}
	Board 5	37^{+18}_{-9}
	Board 6	37^{+35}_{-15}
Step 1	Board 1	26^{+28}_{-10}
	Board 2	33^{+21}_{-9}
	Board 3	37^{+30}_{-12}
	Board 4	35^{+22}_{-11}
	Board 5	54^{+28}_{-24}
	Board 6	33^{+23}_{-10}
Step 2	Board 1	24^{+13}_{-8}
	Board 2	36^{+29}_{-14}
	Board 3	34^{+30}_{-13}
	Board 4	
	Board 5	
	Board 6	34^{+20}_{-9}
Step 3	Board 1	
	Board 2	
	Board 3	29^{+25}_{-11}
	Board 4	54^{+41}_{-17}
	Board 5	
	Board 6	
Step 4	Board 1	
	Board 2	
	Board 3	37^{+30}_{-13}
	Board 4	37^{+45}_{-10}
	Board 5	54^{+49}_{-23}
	Board 6	54^{+33}_{-18}
Step 5	Board 1	
	Board 2	
	Board 3	54^{+13}_{-21}
	Board 4	193^{+162}_{-31}
	Board 5	
	Board 6	
Step 6	Board 1	
	Board 2	
	Board 3	67^{+87}_{-30}
	Board 4	203^{+211}_{-62}
	Board 5	97^{+88}_{-33}
	Board 6	32^{+22}_{-11}
Step 7	Board 1	
	Board 2	54^{+43}_{-19}
	Board 3	103^{+83}_{-35}
	Board 4	
	Board 5	66^{+68}_{-29}
	Board 6	

Table 8: Summary of the corner frequency found for the different noise measurements in the LNA devices.

Table 9 present a summary similar to Tables 7 and 8 corresponding to the *step 8* made at APC.

Step	**Board number**	**Corner frequency (Hz)**	**White noise ($\mu \pm \sigma$)**	
		LNA	**DAC (pA)**	**LNA (nV)**
Step 8	**Board 1**	37^{+26}_{-3}	42 ± 3	0.95 ± 0.07
	Board 2	57^{+27}_{-3}	42 ± 3	0.87 ± 0.07
	Board 3	55^{+10}_{-17}	40 ± 3	0.89 ± 0.07
	Board 4	67^{+35}_{-4}	38 ± 3	1.01 ± 0.07
	Board 5	67^{+30}_{-3}	42 ± 3	1.01 ± 0.05
	Board 6	33^{+21}_{-6}	349 ± 29	0.85 ± 0.05

Table 9: Parameter extraction in *step 8* for all the boards. This measurement was done at APC three month after the annealing of the boards.

9.6 Noise evolution with different dose level

The noise density is analyzed at different frequencies 1 Hz, 10 Hz, 100 Hz, 1000 Hz and compared in all the steps. Tables 10 and 11 summarizes the mean noise density values for the DAC and LNA devices in all the measurement steps, respectively.

Note that in this analysis,data from board 4 is neglected at *steps 5* and *6* (see Figure 29) and also board 1 in *step 7* (see Figure 28) in order to have consistent results. The DAC data in *step 2* is neglected also due to the abnormal behavior of this dataset, as explained in Section 9.2.

Figure 32 shows graphically the data from Table 10 and Figure 33 presents the data from Table 11.

Step	**DAC (pA/$\sqrt{\text{Hz}}$)**			
	1 Hz	**10 Hz**	**100 Hz**	**1000 Hz**
0	1825.2 ± 598.5	502.4 ± 65.1	110.5 ± 7.2	41.5 ± 2.6
1	1642.9 ± 340.8	467.6 ± 48.2	109.0 ± 9.5	40.2 ± 2.6
2				
3	1889.0 ± 348.0	610.5 ± 82.5	161.4 ± 16.3	50.8 ± 3.9
4	1655.7 ± 393.0	505.3 ± 44.5	127.8 ± 12.1	42.0 ± 2.8
5	1259.6 ± 330.5	413.9 ± 45.1	111.2 ± 13.9	38.0 ± 2.6
6	1620.8 ± 432.7	542.5 ± 95.2	104.5 ± 18.4	37.1 ± 3.4
7	1411.1 ± 319.1	477.348 ± 71.3	118.1 ± 14.5	40.9 ± 3.2
8	1511.0 ± 388.8	463.4 ± 22.0	113.9 ± 4.8	38.9 ± 1.3

Table 10: Evolution of the DAC noise over frequency in all the measurement steps. Average noise obtained over all the boards in all the steps.

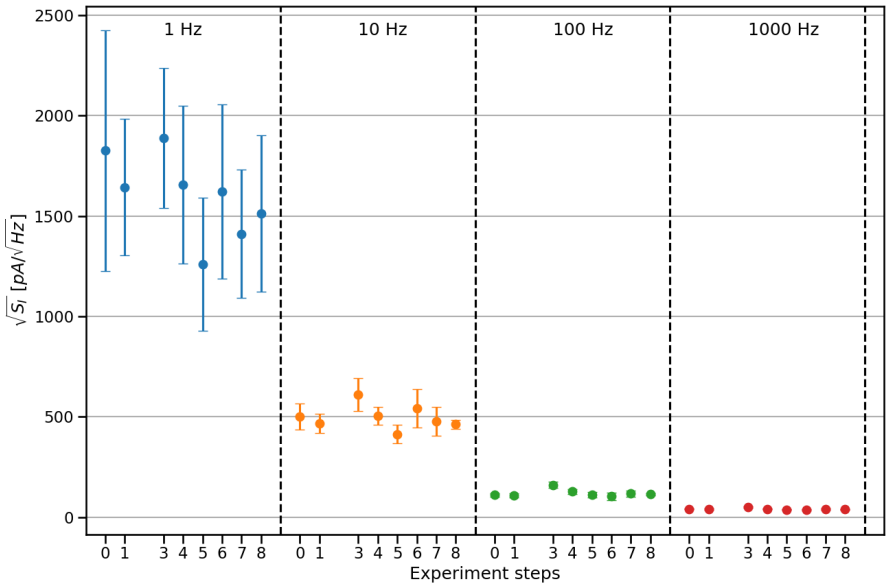

Figure 32: Evolution of the DAC noise over frequency in all the measurement steps.

Step	**LNA (nV/$\sqrt{\text{Hz}}$)**			
	1 Hz	**10 Hz**	**100 Hz**	**1000 Hz**
0	4.66 ± 1.16	1.65 ± 0.12	1.08 ± 0.06	0.86 ± 0.04
1	3.48 ± 0.79	1.57 ± 0.12	0.93 ± 0.09	0.86 ± 0.04
2	3.32 ± 1.09	1.39 ± 0.09	0.86 ± 0.07	0.83 ± 0.05
3	3.33 ± 0.71	1.82 ± 0.24	0.98 ± 0.16	0.83 ± 0.08
4	4.66 ± 0.77	1.69 ± 0.17	0.94 ± 0.10	0.84 ± 0.05
5	4.50 ± 1.24	2.64 ± 0.35	0.99 ± 0.19	0.87 ± 0.06
6	5.64 ± 1.72	2.45 ± 0.28	1.09 ± 0.18	0.91 ± 0.06
7	6.03 ± 1.61	2.42 ± 0.36	0.93 ± 0.15	0.86 ± 0.06
8	5.16 ± 1.29	2.09 ± 0.11	1.08 ± 0.02	0.91 ± 0.02

Table 11: Evolution of the LNA noise over frequency in all the measurement steps. Average noise obtained over all the boards in all the steps.

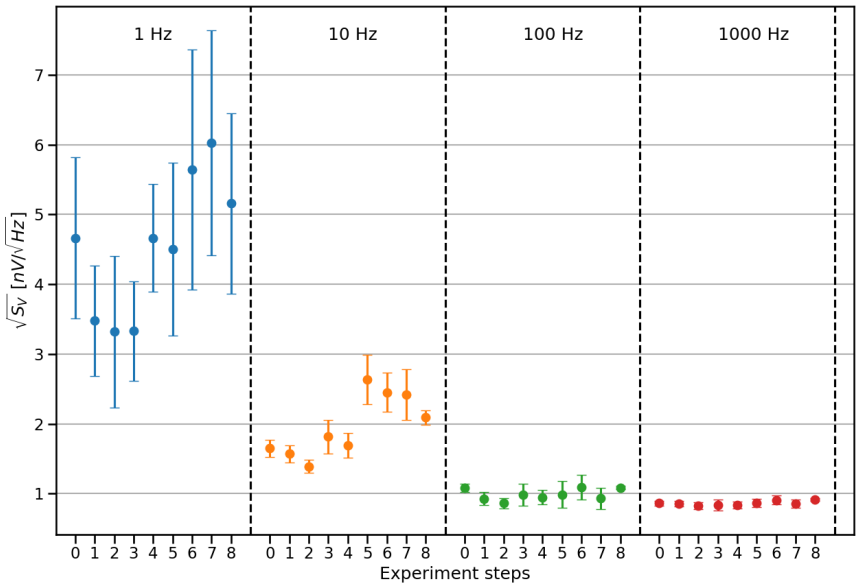

Figure 33: Evolution of the LNA noise over frequency in all the measurement steps.

10 Biased vs not-biased

Analyzing the data in Section 8 and Section 9 there are no appreciable effects on the discrete devices of the ASIC due to the fact the boards were biased or not in the measurement. There are no correspondence between the changes in the noise level observed of the boards and the bias status of the same boards.

11 Conclusions

The total dose level started at 6 krad and ended at 200 krad for some ASICs, according to the Table 1 and to the AD-01 document. Some of the irradiation steps with total dose levels were superior to the nominal mission values requirements in order to test the AwaXe_v4 ASIC over extreme conditions.

The status of all the boards after the irradiation process was verified in terms of power consumption, capacitance of the MIM capacitor, gain of the LNAs and functionality of the DACs. The values of power consumption were similar to the values reported in the RD-03. This results shows small or null changes in the power consumption of the boards, indicating a good health of the analog devices in the ASIC after the irradiation process. This hold true even for boards that have received the highest radiation doses.

The internal components of the ASIC were tested in low-current regime to observe the effects of irradiation since otherwise these effects would be very difficult to distinguish, especially in the working region with nominal currents for these devices. From the analysis of these results, there are no appreciable effects on the discrete devices internal to the ASIC due to the radiation dose levels applied.

It is important to mention, however, the fact that the β parameter of the NPN transistors is affected by dose. This parameter shows a change of the order of $\sim$55% going down in value, being one of the most affected parameters in all the measurements. However, after the annealing process there

is a small recovering, reaching a ∼40% of the original value. As mentioned, these effects occurs in the low-current regime and we do not observe changes in the nominal current regime of the mission.

After all the irradiation procedure, noise measurements were performed to all boards to check the status of the LNA and DAC devices. The noise level, after three month of the Germany measurements, is similar for all the devices and there are no observable effects over the noise density of these devices due to the total dose tests.

The complete noise path is reported up to the measurement instrument in the setup. This was useful to identify all the noise contributions in our measurement setup.

It was necessary to filter the dataset in order to maintain only the ones having some physical meaning. With this data it was possible to obtain for the DACs an average white noise density of $43 \pm 7\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ and for the LNAs an average white noise density of $0.9 \pm 0.1\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$. This is valid in the frequency range 300 Hz to 1000 Hz.

The noise evolution was considered over all the frequency range of the measurements and the corner frequency was obtained for the LNA devices. In general, most of the corner frequencies obtained are distributed within the range from 20 Hz to 80 Hz.

There is not an observable correspondence between the changes in the noise level of the boards and the bias status of the same boards. The same apply for the internal discrete devices of the ASIC.

A Operating point plots for all the boards

A.1 Current Mirror

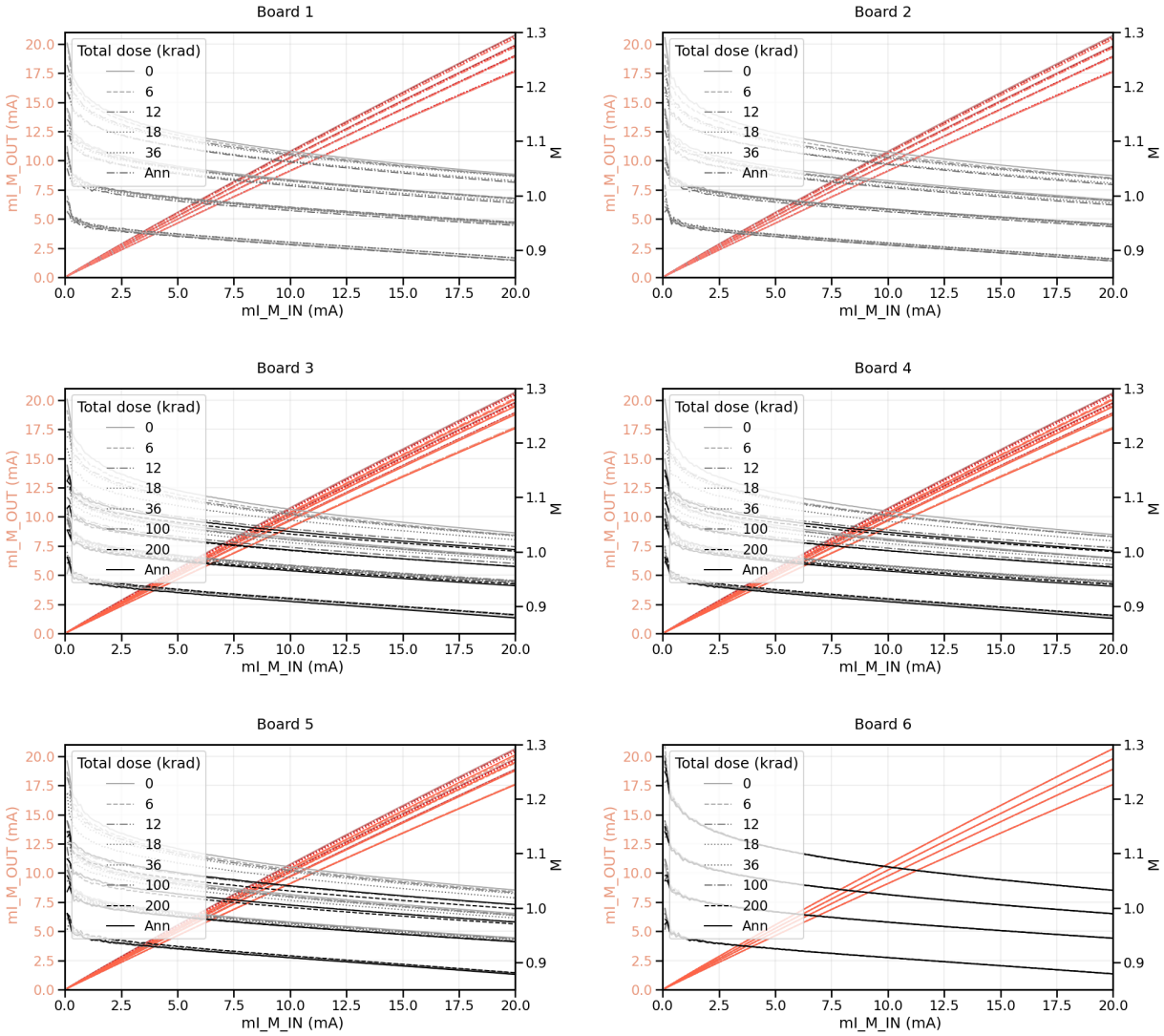

Figure 34: Mirror plot for the 6 boards.

A.2 NPN1 GP

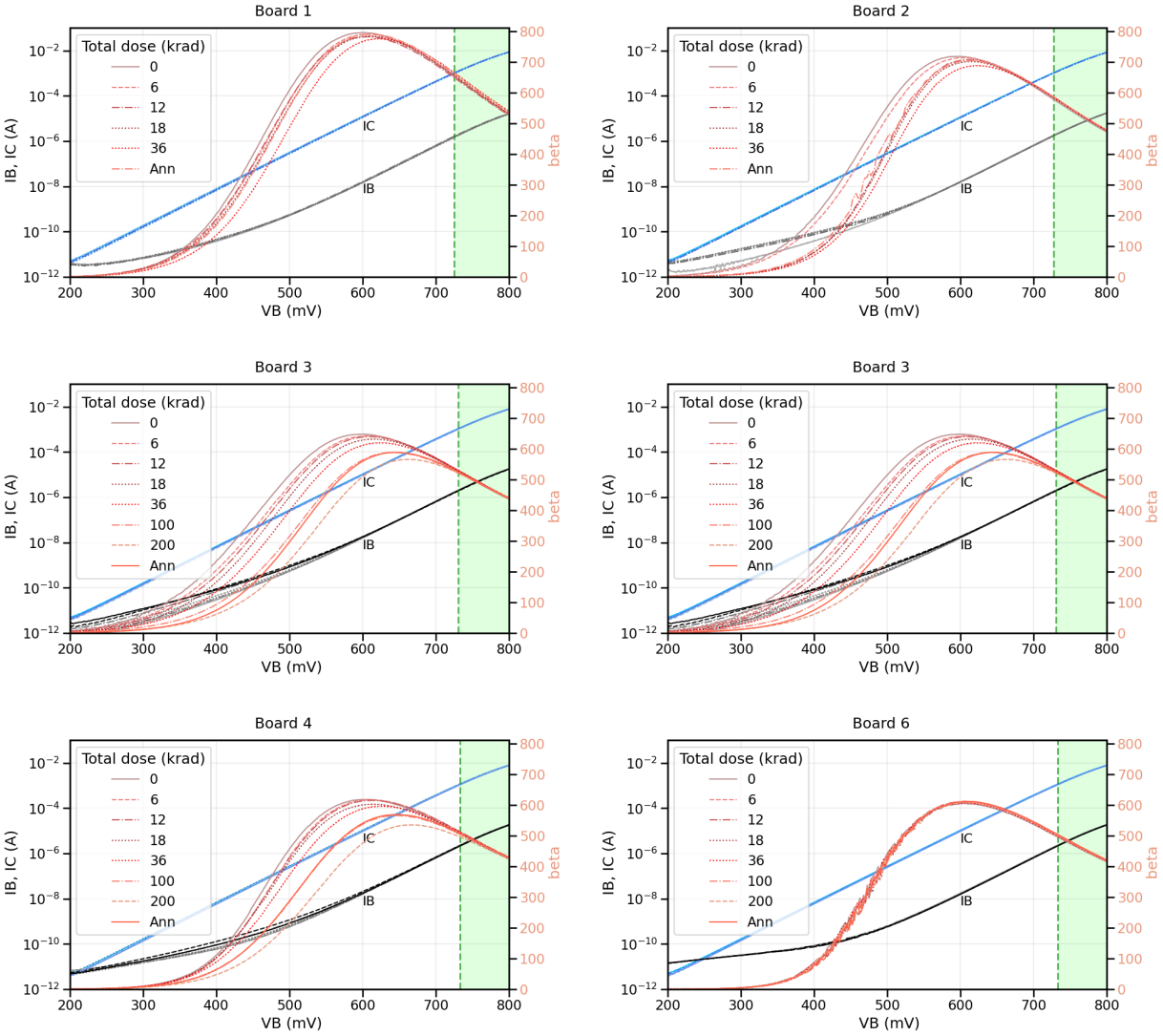

Figure 35: Gummel plot for the NPN1 device in the 6 boards.

A.3 NPN1 IC VCE

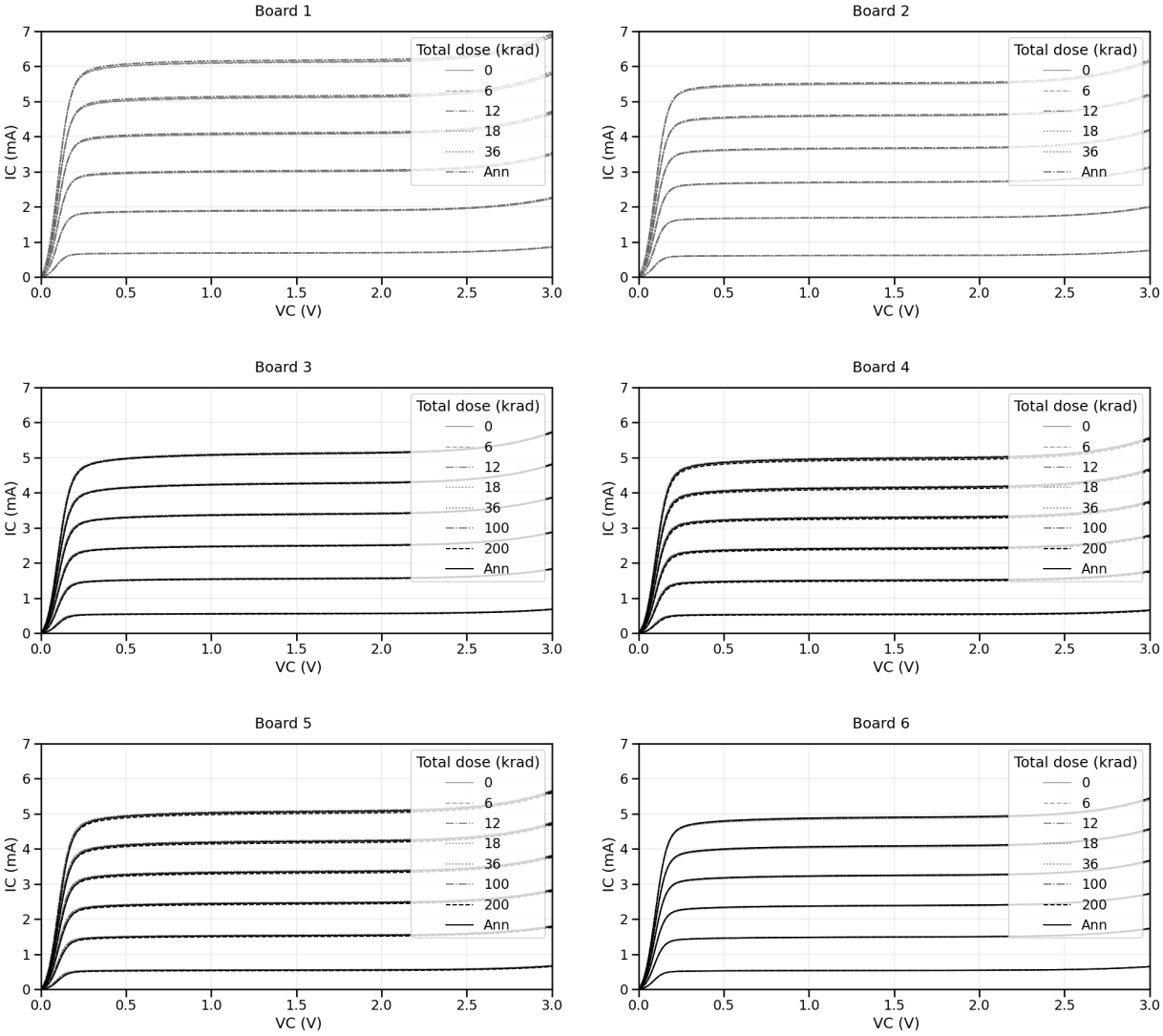

Figure 36: I_b and I_c vs V_{ce} plot for the NPN1 device in the 6 boards.

A.4 NPN2 GP

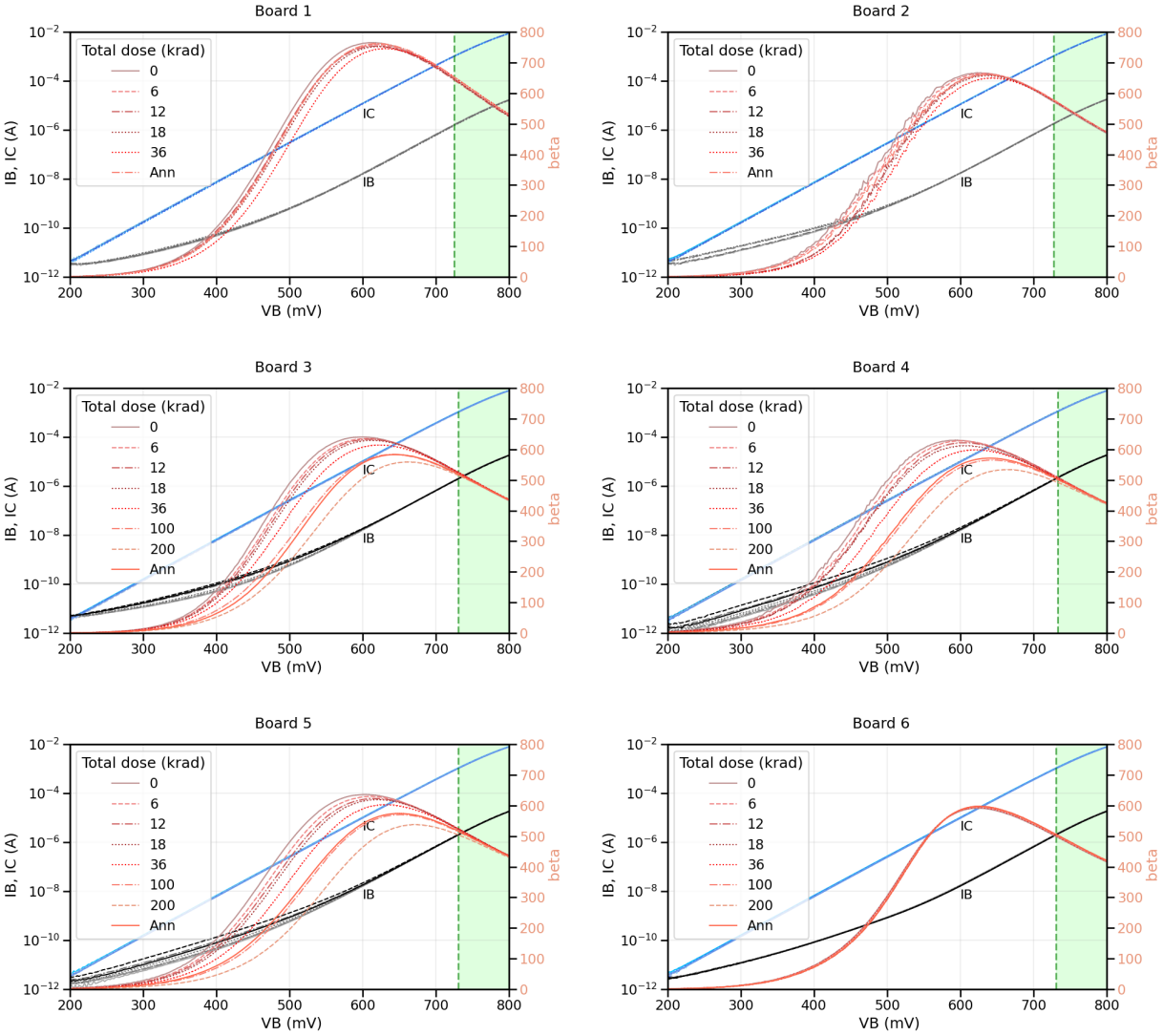

Figure 37: Gummel plot for the NPN2 device in the 6 boards.

A.5 NPN2 IC VCE

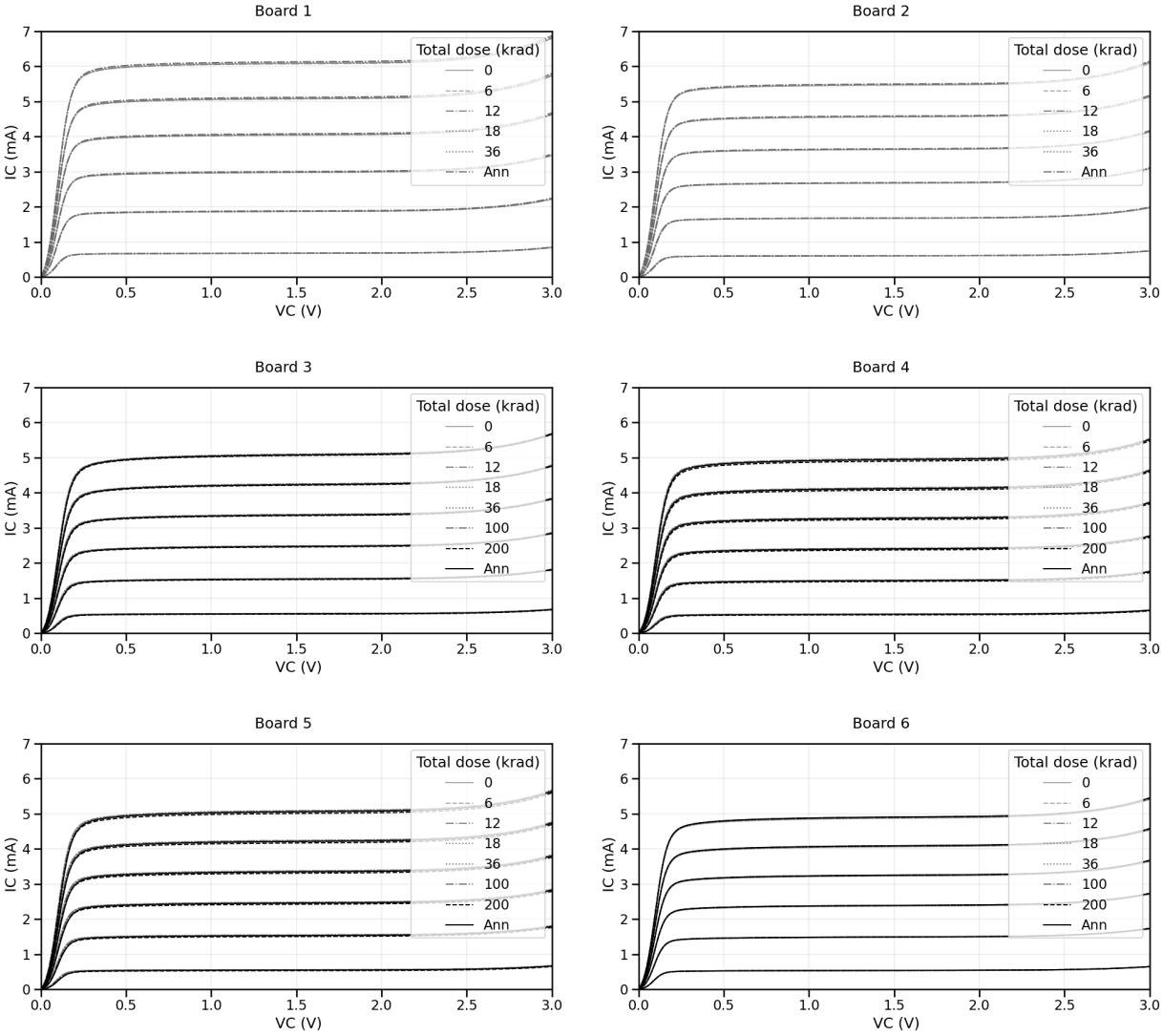

Figure 38: I_b and I_c vs V_{ce} plot for the NPN2 device in the 6 boards.

A.6 PNP GP

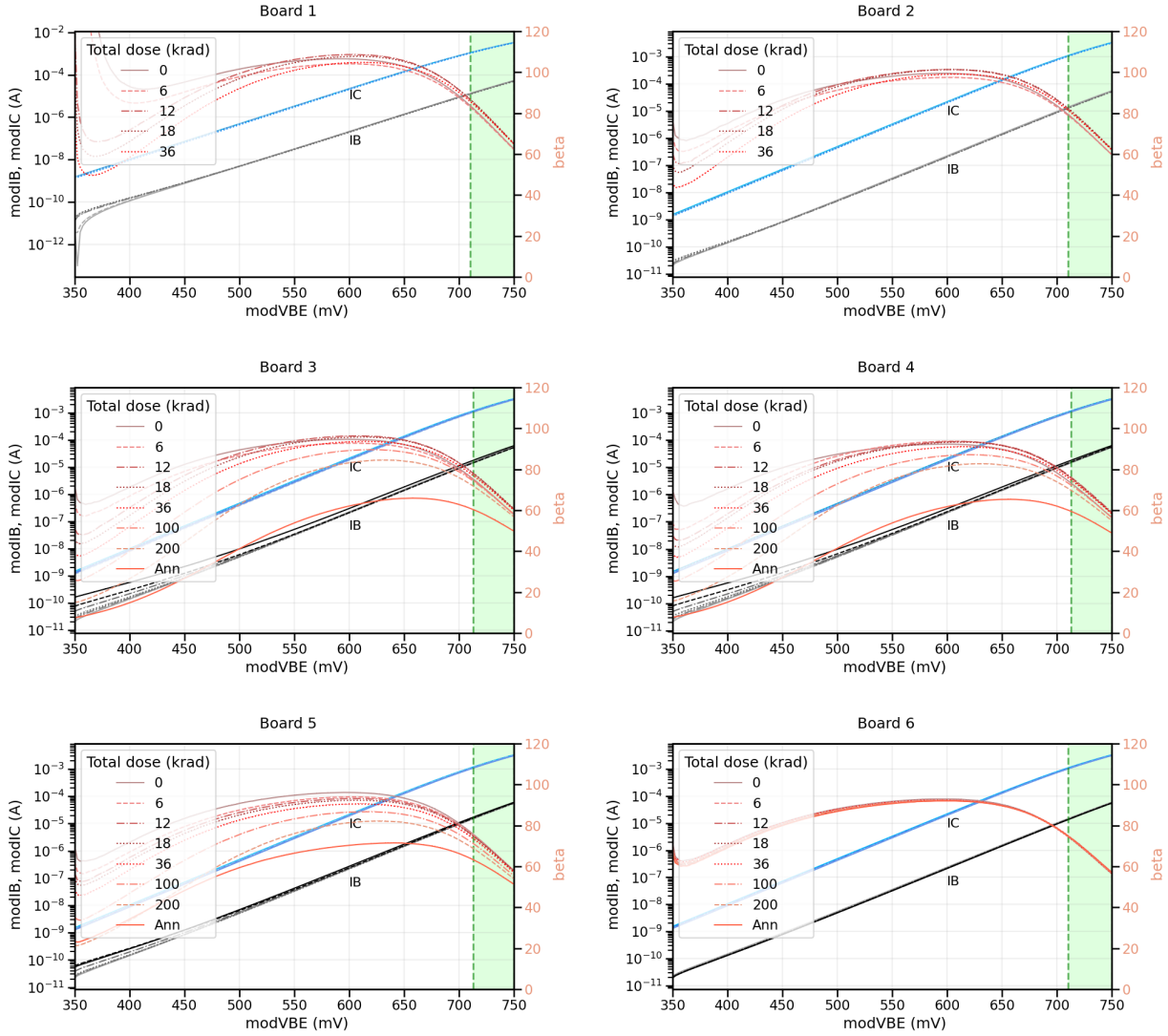

Figure 39: Gummel plot for the PNP device in the 6 boards.

A.7 PNP IC VCE

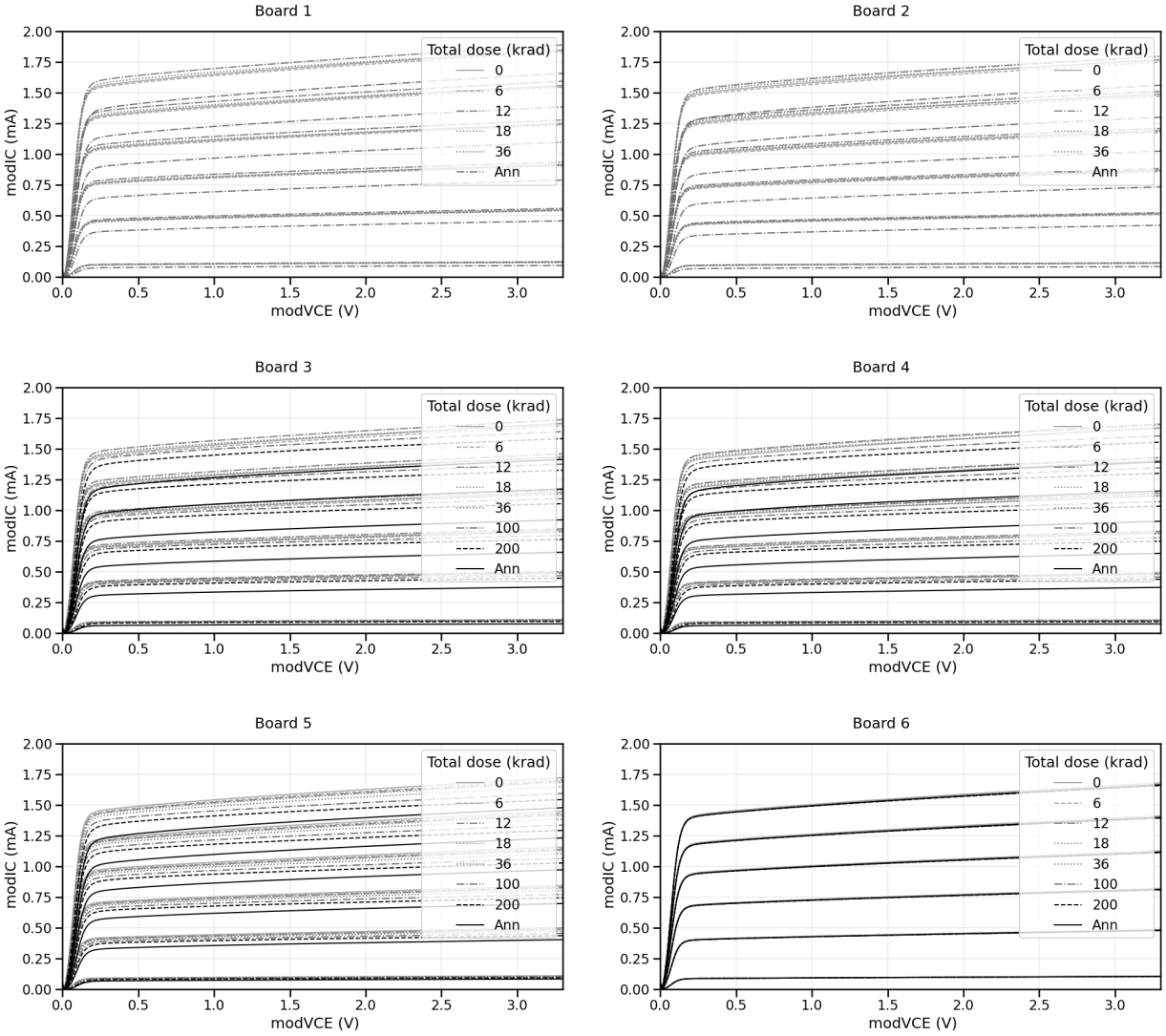

Figure 40: I_b and I_c vs V_{ce} plot for the PNP device in the 6 boards.

A.8 NMOS1 ID VGS

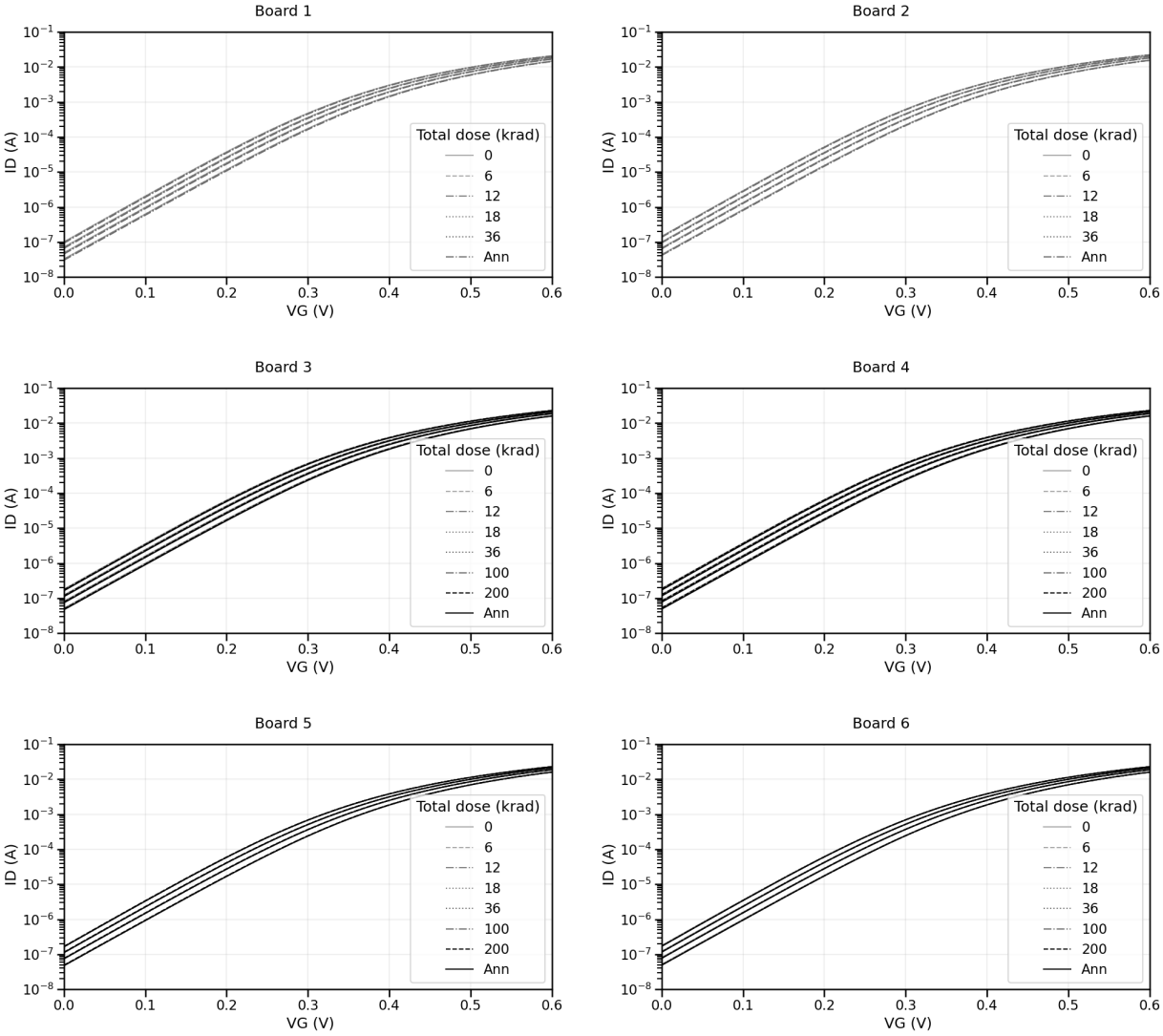

Figure 41: I_d vs V_{gs} plot for the NMOS1 device in the 6 boards.

A.9 NMOS1 ID VDS

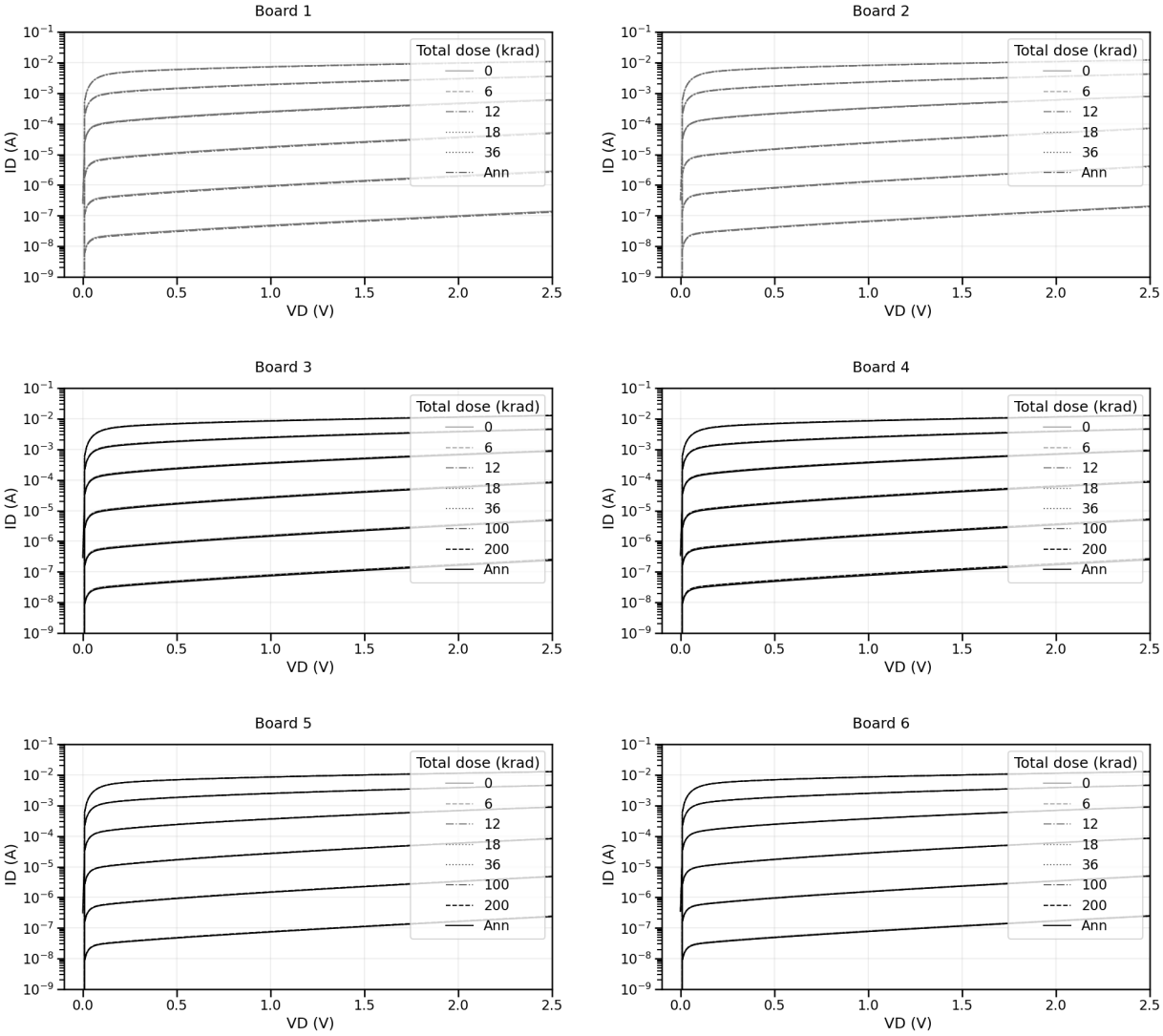

Figure 42: I_d vs V_{ds} plot for the NMOS1 device in the 6 boards.

A.10 NMOS2 ID VGS

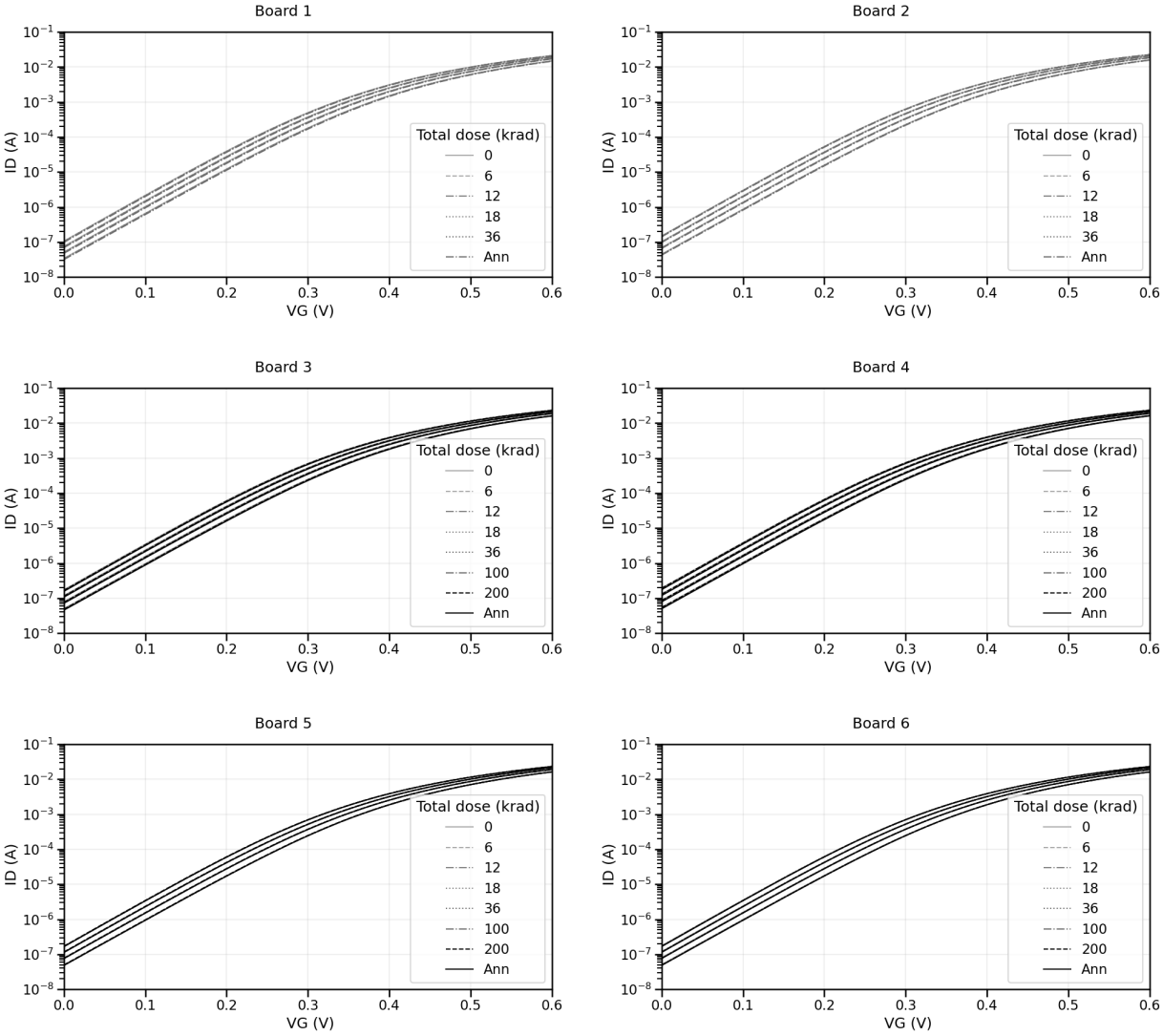

Figure 43: I_d vs V_{gs} plot for the NMOS2 device in the 6 boards.

A.11 NMOS2 ID VDS

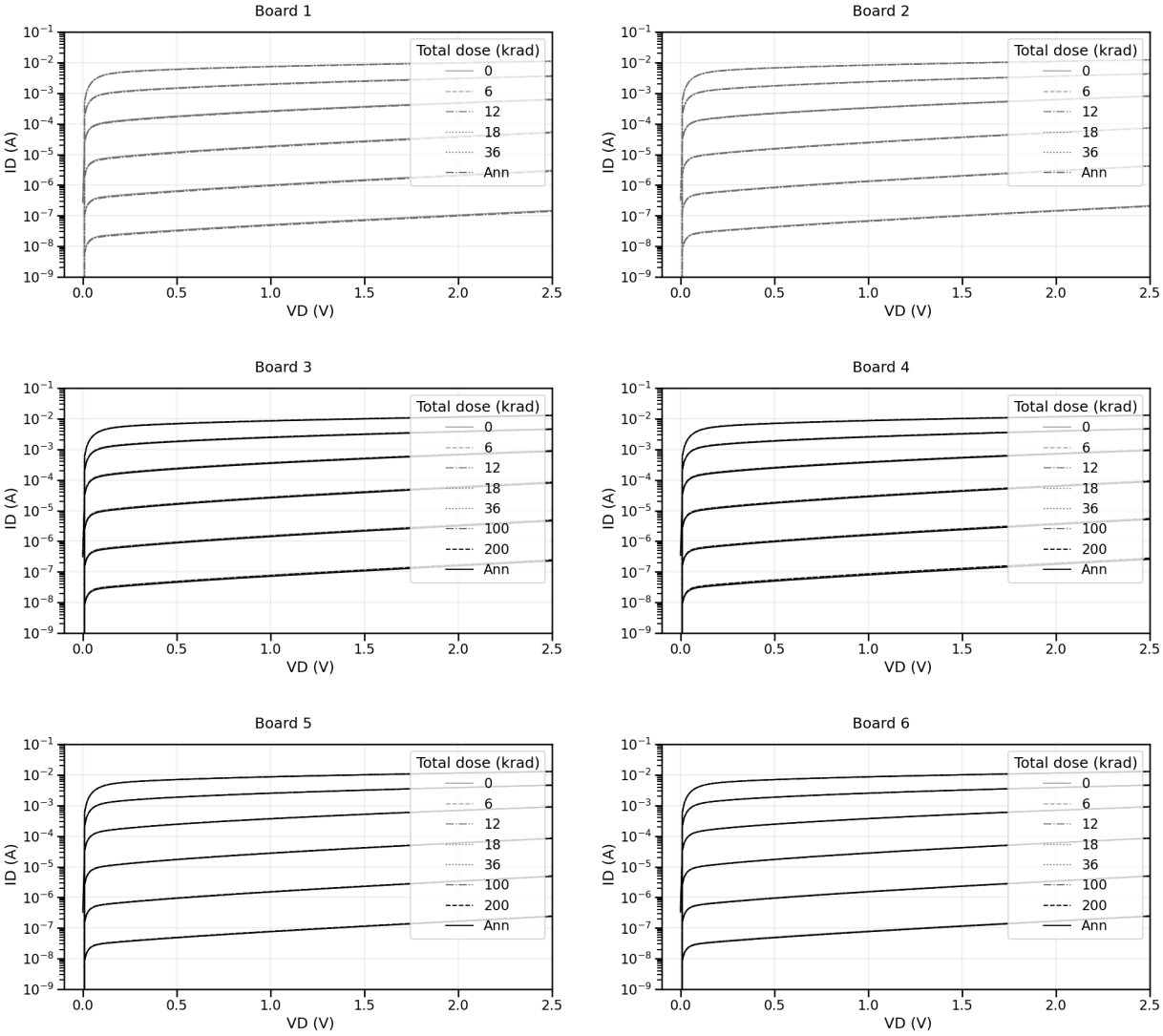

Figure 44: I_d vs V_{ds} plot for the NMOS2 device in the 6 boards.

A.12 PMOS ID VGS

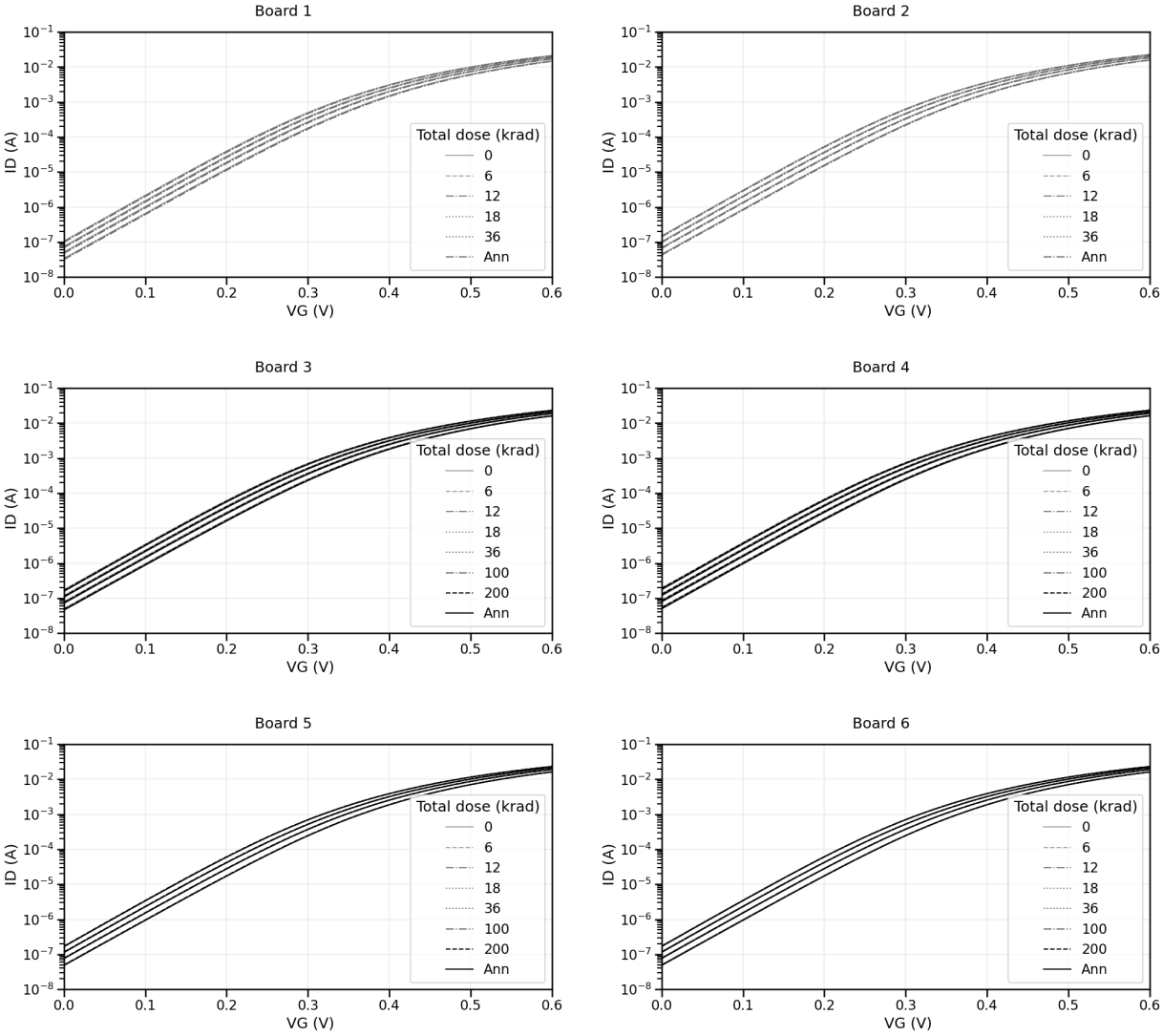

Figure 45: I_d vs V_{gs} plot for the PMOS device in the 6 boards.

A.13 PMOS ID VDS

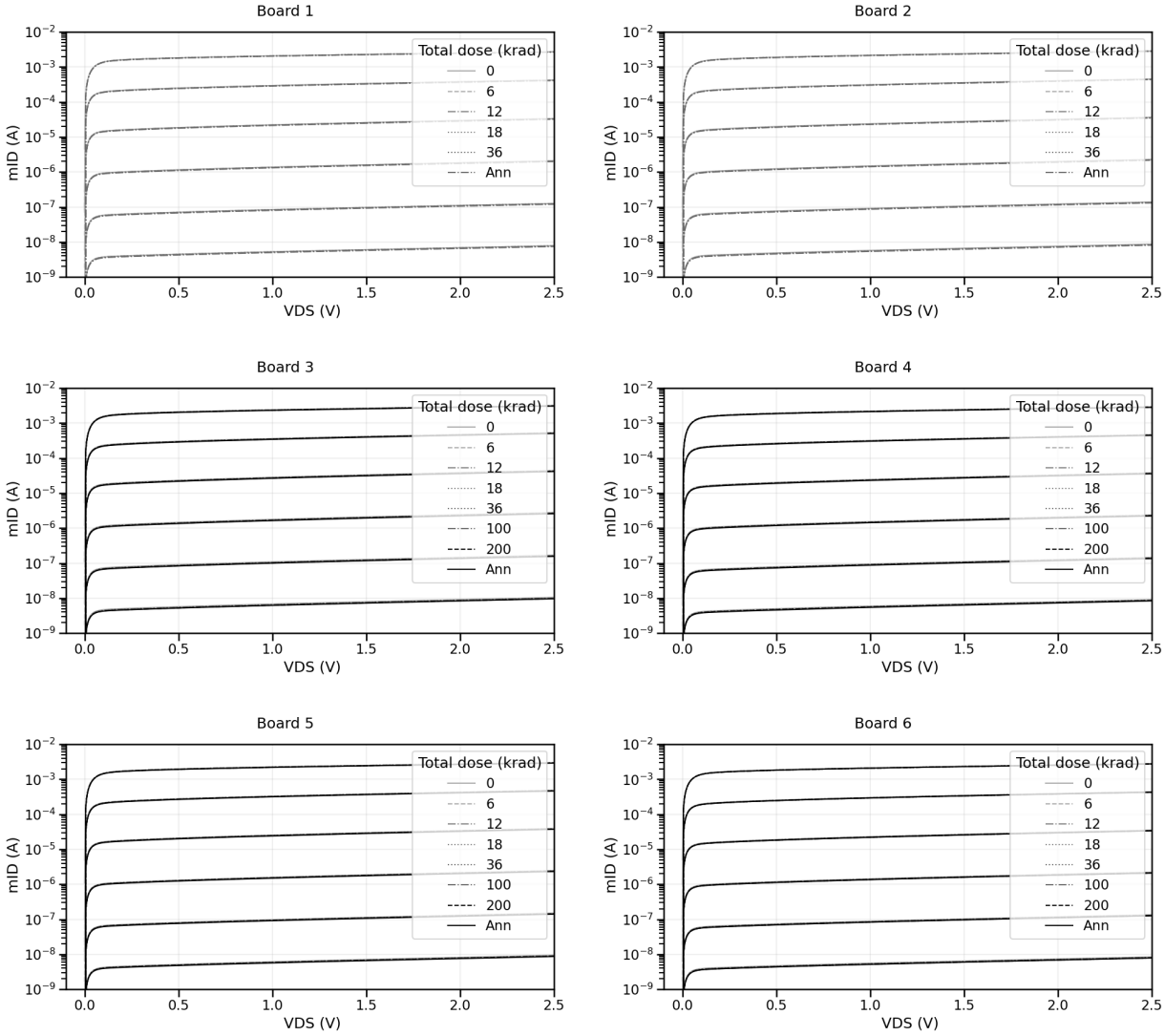

Figure 46: I_d vs V_{ds} plot for the NMOS2 device in the 6 boards.

A.14 C leakage

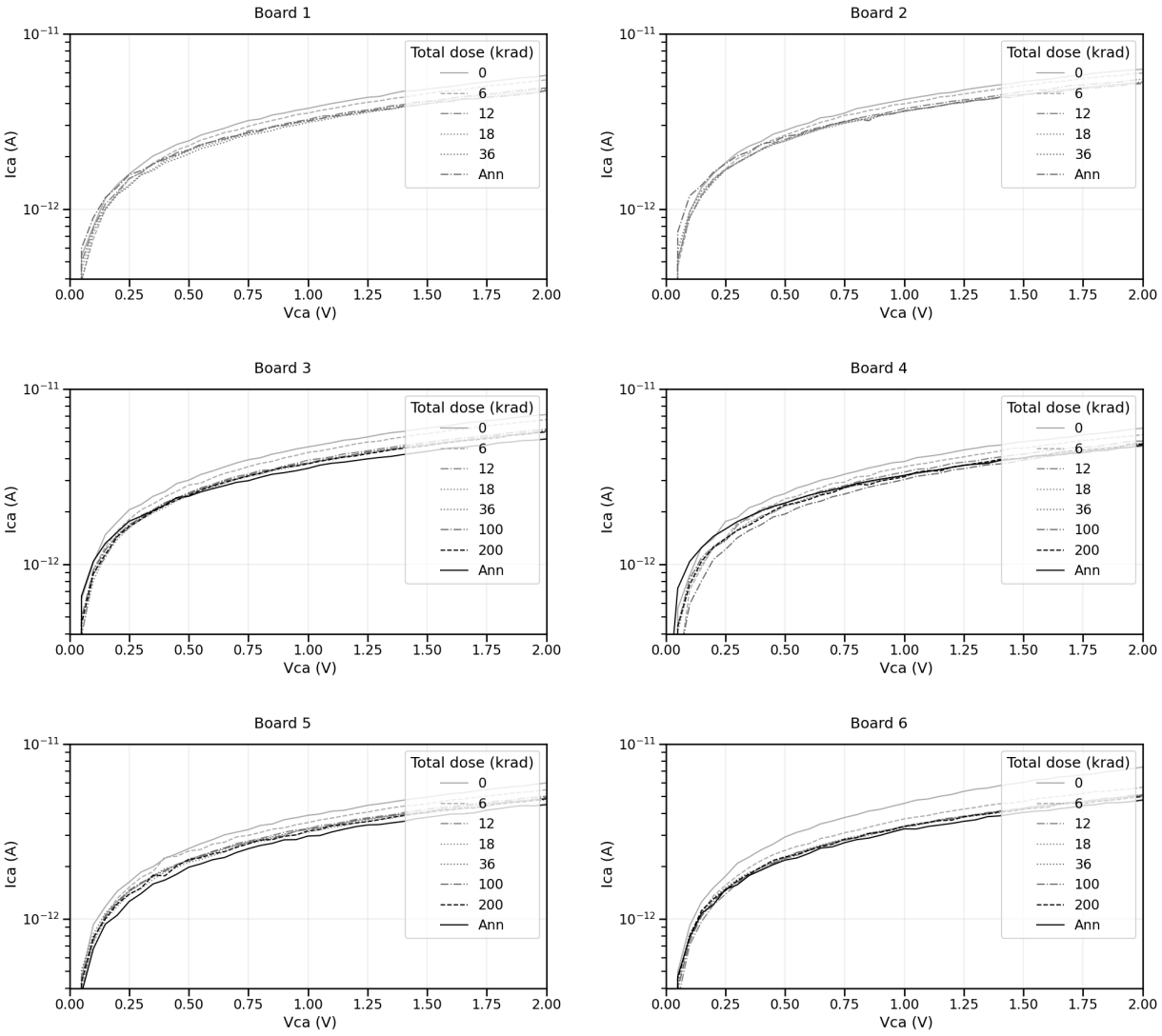

Figure 47: C leakage in the 6 boards.

B Noise dataset for all the boards

B.1 DAC measurements

B.1.1 Low frequency range (from 1 Hz to 100 Hz)

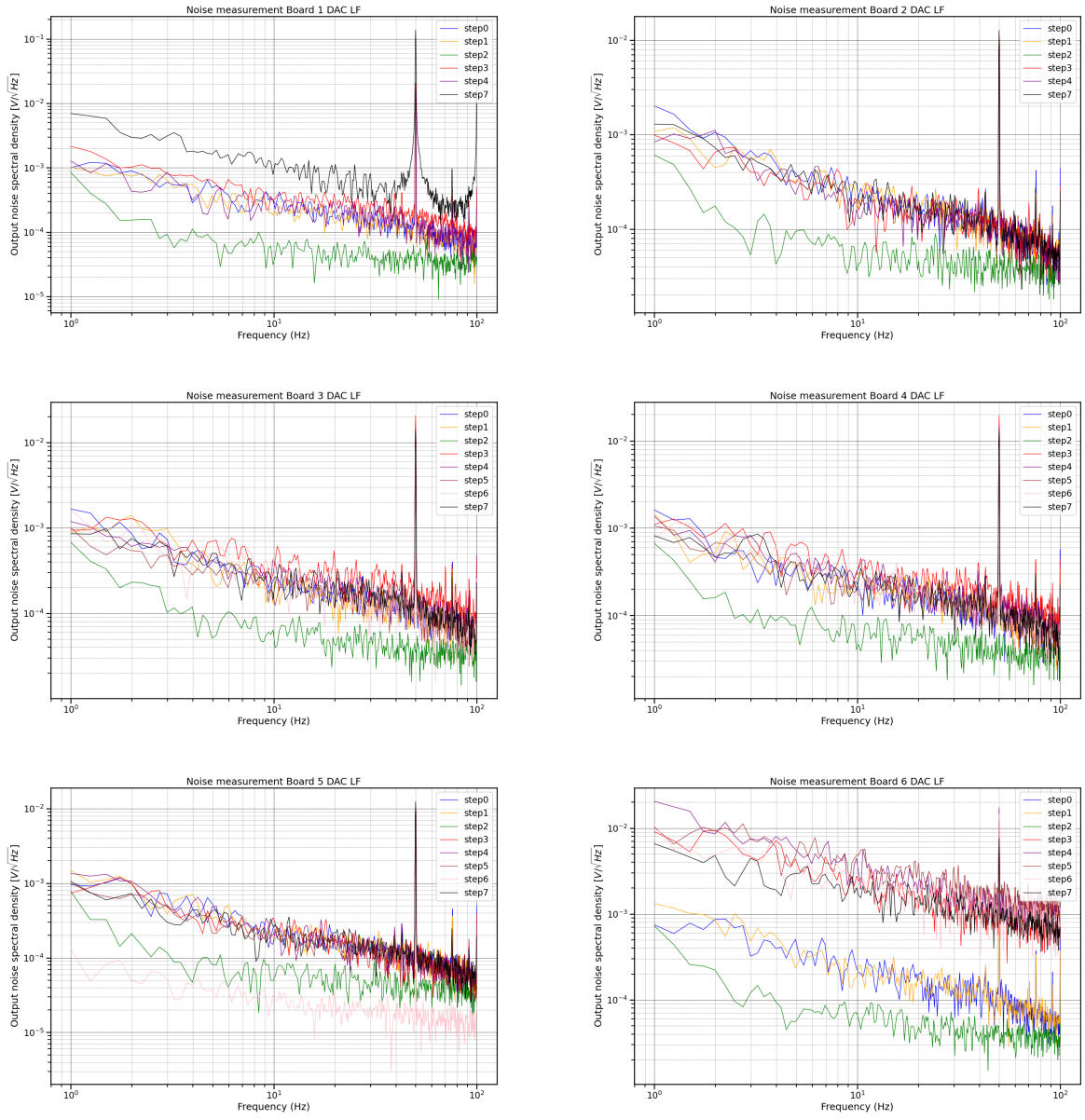

Figure 48: Output noise of the DAC measurements in the frequency range from 1 Hz to 100 Hz. Raw data, not taking into account the gains/losses in the measurement setup.

B.1.2 High frequency range (from 10 Hz to 1000 Hz)

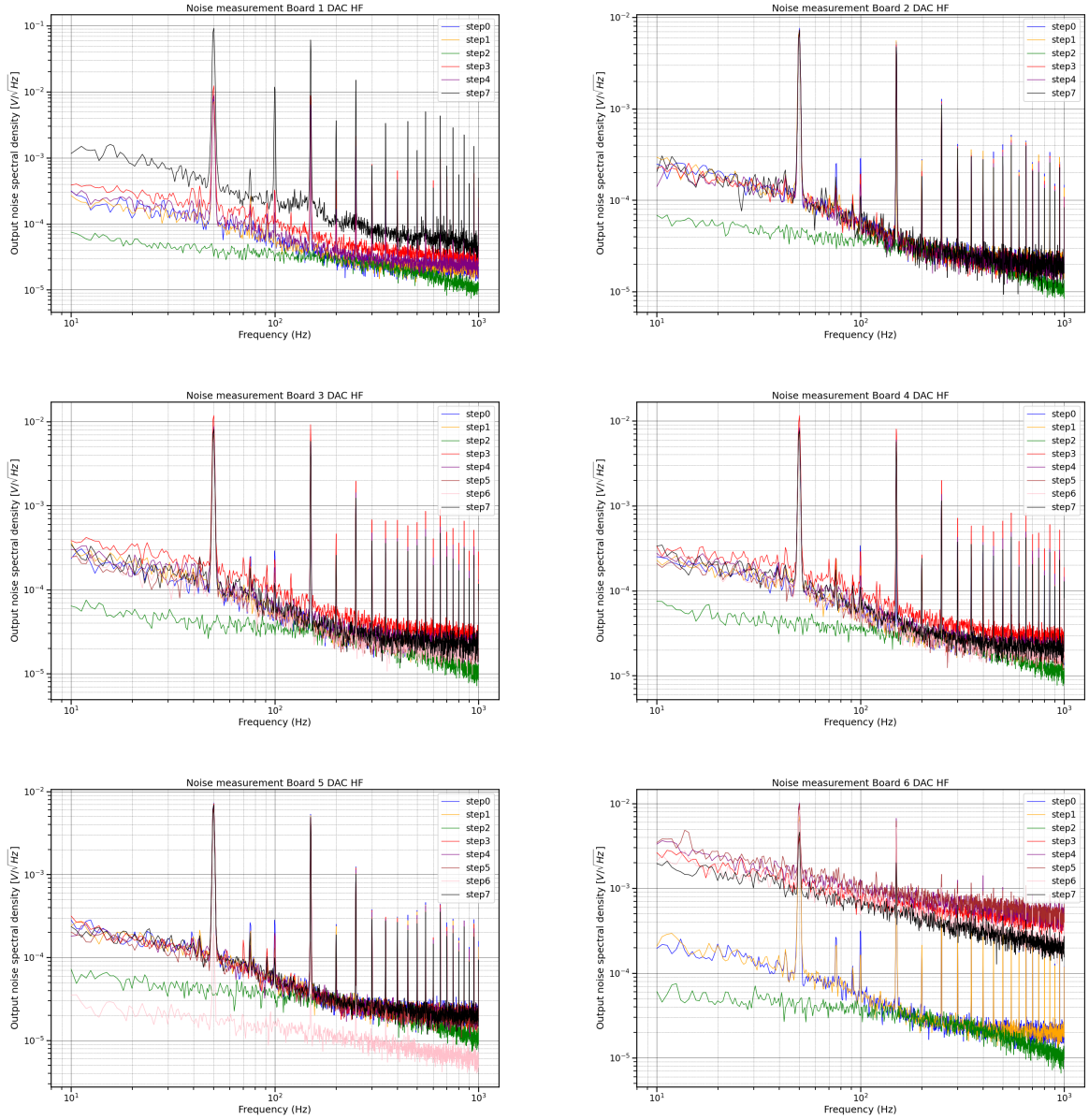

Figure 49: Output noise of the DAC measurements in the frequency range from 10 Hz to 1000 Hz. Raw data, not taking into account the gains/losses in the measurement setup.

B.2 LNA measurements

B.2.1 Low frequency range (from 1 Hz to 100 Hz)

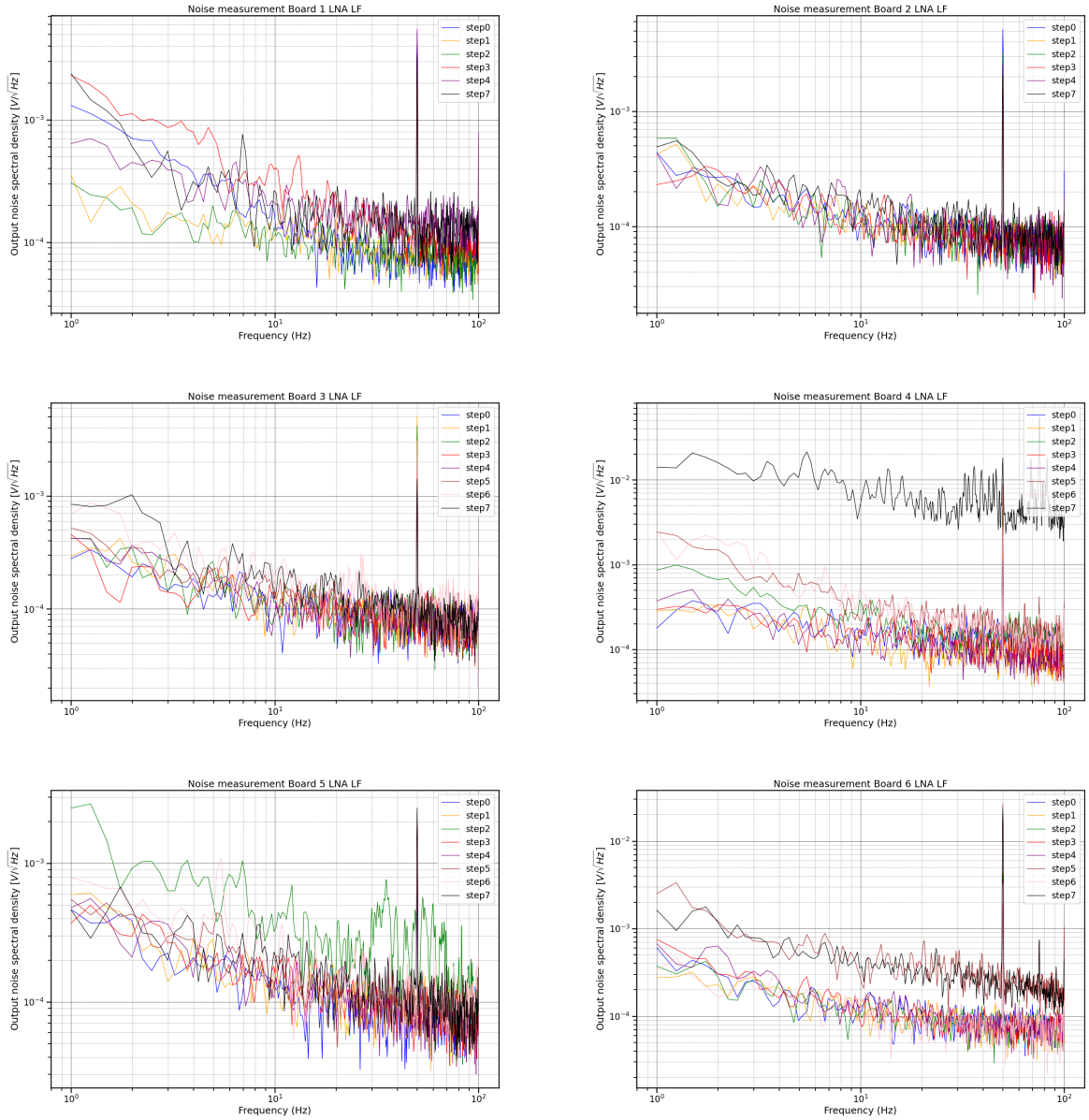

Figure 50: Output noise of the LNA measurements in the frequency range from 1 Hz to 100 Hz. Raw data, not taking into account the gains/losses in the measurement setup.

B.2.2 High frequency range (from 10 Hz to 1000 Hz)

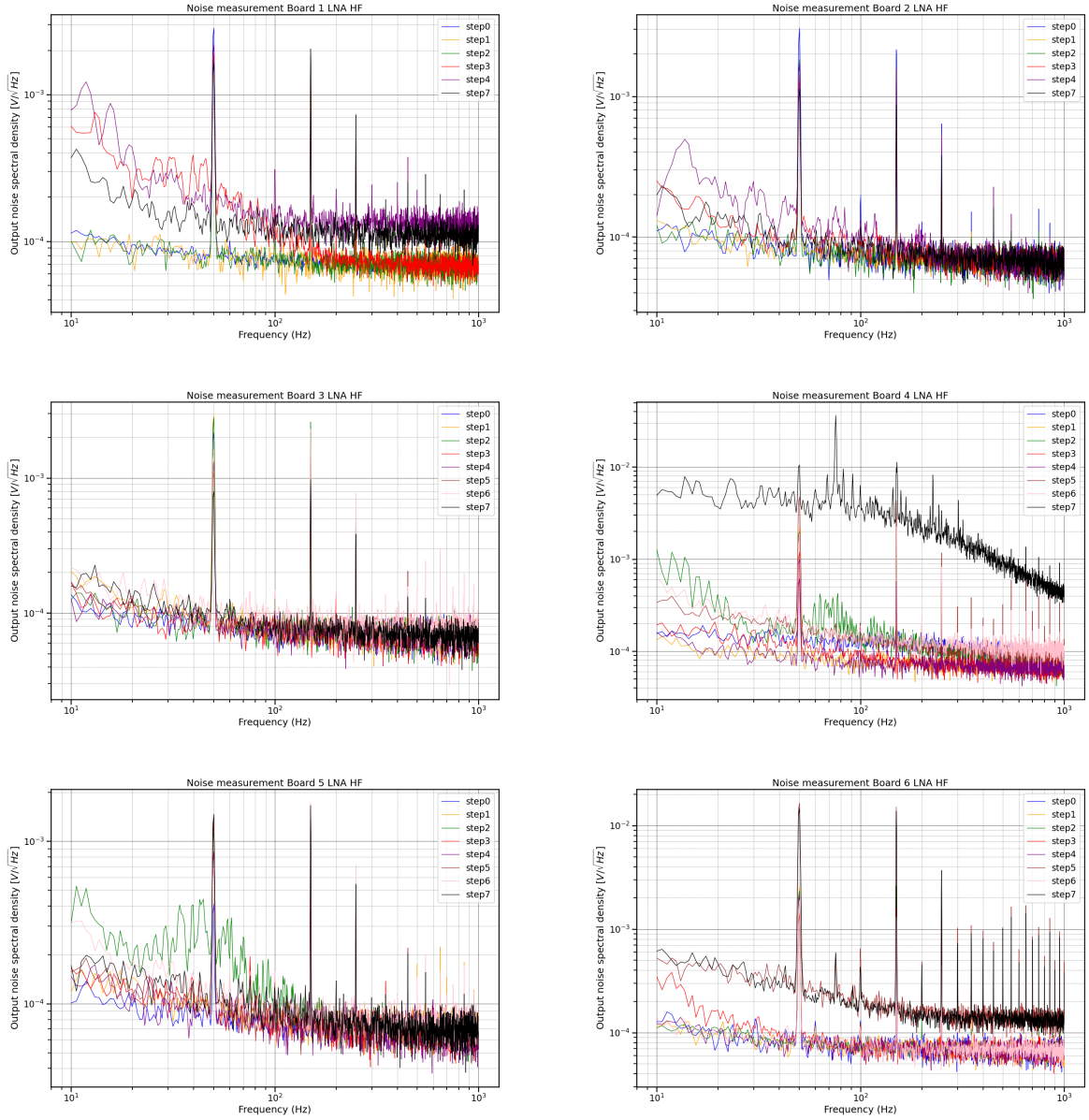

Figure 51: Output noise of the LNA measurements in the frequency range from 10 Hz to 1000 Hz. Raw data, not taking into account the gains/losses in the measurement setup.